The CSI Journal on
Computer Science and Engineering
Vol. 10, No. 2 & 4 (b), 2012
Pages 1-9
Regular Paper

A New Tri-State Based Static Random Access Memory with Improved Write-Ability and Read Stability

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Abstract

In this paper, we have presented a new design for Static Random Access Memory Cell. In our first improvement, we add one PMOS and one NMOS transistor to conventional 6T SRAM cell leading to 8T cell. In this way, we improve the performance of cell. However, we reduce the overhead of area by sharing the added two transistors among four cells in the same row of an SRAM array, so we obtain an equivalent 6.5T cell. These extra transistors help to improve write-ability by breaking the feedback of back to back inverters during write operation. By mean of this innovation, we obtained improvement in Write Noise Margin (WNM) by 60\% over conventional 6T cell which approves efficiency of our approach. Proposed 8T SRAM cell also reduces leakage power and active power for single write operations by 15% and 54% over 6T design at supply voltage of 500mV. To consider further scaling, proposed 8T SRAM cell is redesigned using 16nm PTM Bulk-CMOS and Fin FET transistors. Simulations with this condition show considerable improvement in Read Static Noise Margin (RSNM) and Hold SNM (HSNM) for Fin FET-based-cell. Finally, a 32kb SRAM using the proposed scheme is designed in a 90nm industrial CMOS technology. Detailed simulations also predict that at supply voltage of 800mV, read and write powers per operation of our design will be 0.36pJ and 7.5pJ, respectively and it is operational at frequencies as high as 1.43GHz.

Keywords: Bulk CMOS, Fin FET, Low Power Design, Memory, Sub Threshold, Sense Amplifier, Static Random Access Memory (SRAM).

1. Introduction

RAMs are one of the most important blocks in modern chips and consume a large part of area and power of a chip [1]. Therefore, reducing the area and power consumption of SRAMs will directly translate to improvement in total area and power of the chip. One effective solution to reduce power consumption is reducing supply voltage of the chip [2]. But reduced Read Static Noise Margin (RSNM) and narrow Write Noise Margin (WNM) due to effects of fabrication process variations, would not allow the successful operation of conventional 6T SRAM at supply voltages bellow 0.7V in a 90nm technology [3].

A good solution to compensate the malfunction of conventional 6T SRAM cell at low voltages is used in [4] where functionality is improved by separating the access transistors responsible for read and write operations; this goal is reached by adding two transistors to conventional 6T cell and use of buffering for read operation. The main problem in design used in [4] is leakage through transistors connected to read bit-lines which limits the maximum possible number of cells integrated in a single column and results in lower density of SRAM block. Several methods were proposed to reduce the leakage current through bit-lines. Authors in [5] and [6] used 10T SRAM cells. In these cells two extra transistors were added to the read path that help to reduce leakage current through read path between cell and read bit-line. Authors in [7] also separated the read/write bit-lines and used a read buffer. They also used a charge-pump circuit to provide a voltage two times larger than VDD and applied it to the source of an NMOS transistor in the read buffer for non-accessed cells which resulted in capability of

integrating 256 cells in a single column. In this paper, we proposed a new tri-state based design for SRAM cell and also integration of cells in an array. Proposed design improves write-ability and read stability over conventional 6T design, while consumes lower leakage in idle mode and active power for write operation.

The rest of this paper is organized as follows. In Section II, we consider and describe some challenges of using conventional 6T SRAM cell in sub-threshold region, Section III introduces our proposed 8T SRAM cell. The simulation results for our proposed design are presented in Section IV. Section V shows the great effects of using Fin FET transistors on improving the SNM for our proposed design. In Section VI, integration of the proposed cell in an SRAM array is described. Finally, Section VII concludes the manuscript.

2. SRAM Cell Challenges in Sub-Threshold Region

At low supply voltages, 6T SRAM cell functionality is impaired. This disorder generally includes one of the issues of write failures, read failures, and low noise margins while reading and maintaining the data [8]. In the following subsections, these challenges are discussed.

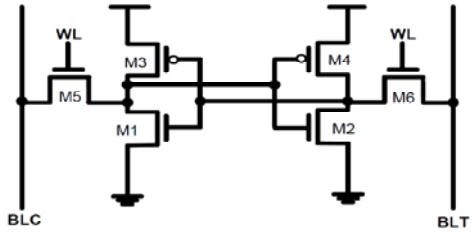


Figure 1. Conventional 6T SRAM cell

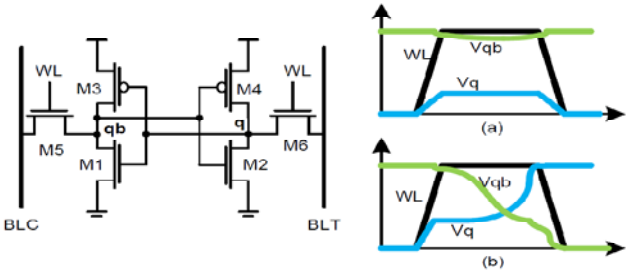


Figure 2. Illustration of (a) successful and (b) unsuccessful read operations in a convertional 6T cell [8]

2.1. Unsuccessful Write Operation in Conventional 6T SRAM Cell

Write failure occurs when correct data cannot be written in storage cells. In reality, due to strong feedback effect of back-to-back transistors, with a weak access transistor, writing data correctly would be challenging and in many cases impossible. As depicted in transistor-level schematic of conventional 6T SRAM cell in figure 1, to have a successful write operation, size of access transistors M5 and M6 must be greater than PMOS transistors of back-to-back inverters M3 and M4. In the next sub-section, we describe the situation for unsuccessful read operation.

2.2. Unsuccessful Read Operation in Conventional 6T SRAM Cell

Unsuccessful read operation occurs when stored data in the cell changes during read operation. To be more precise, top right graph in figure 2 shows the successful read operation where the voltages Vqb and Vq maintain their values and do not flip, or in other words Vqb stays higher than Vq during reading operation. However, the bottom right graph in figure 2 shows that in the reading operation, when word-line signal WL goes high, voltage Vq starts rising and at the end of the operation the Vq node flips and falsely becomes high. Obviously, this is an undesired situation causing corruption in the stored value of the cell.

Figure 3 shows the probability of read and write failures versus supply voltage for conventional 6T cell. To prevent the flipping problem, size of access transistors must be as small as possible but in other hands, for successful write operation, size of access transistors cannot be very small.

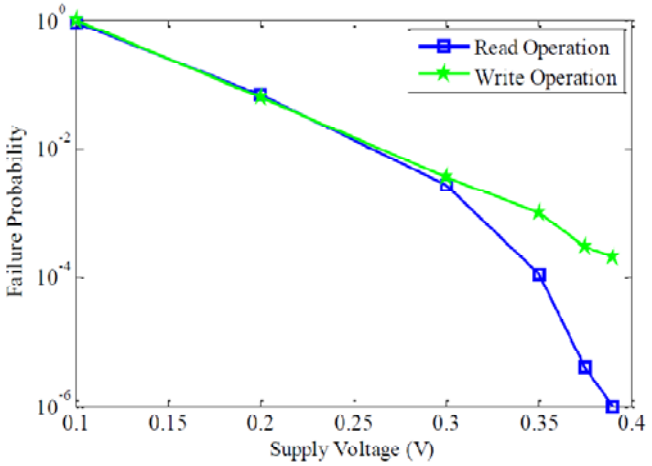


Figure 3. Read/Write failure probability of conventional 6T cell versus VDD

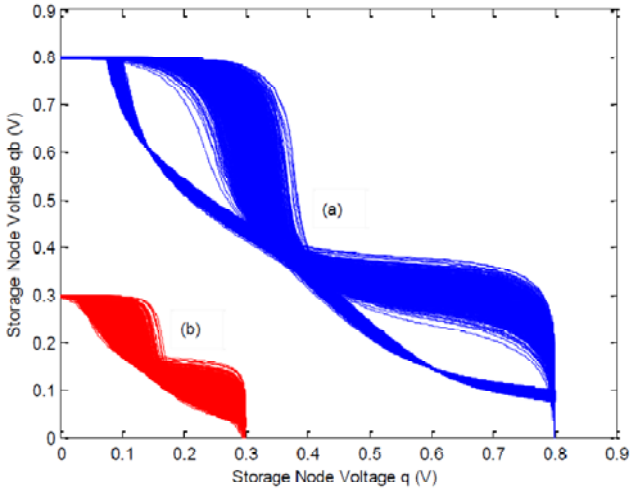


Figure 4. Read butterfly plot of conventional 6T SRAM cell at supply voltages of (a) 800mV, and, (b) 300mV, in presence of process variation

This is the dilemma of access transistor sizing in conventional 6T cell. That is if we choose large ones, the

reading operation will be unsuccessful and if we choose small ones, the writing operation might become unsuccessful.

2.3. Low Read SNM for Conventional 6T SRAM Cell

Conventional 6T SRAM cell has good Hold SNM but it suffers from very low SNM for Read especially at low voltages. Standard procedure to get SNM of SRAM cells is to plot its butterfly diagram while considering possible environment and process variations that might occur during device's operation and try to place the biggest possible square in the butterfly; dimensions of the square will be SNM of that particular cell for the particular operation. Clearly, if two sides of curves in a butterfly diagram do not meet, there exist some SNM, but if these sides meet together, the SNM will be zero. Figure 4 shows the butterfly diagram of conventional 6T SRAM cell at 800mV and 300mV supply voltages, which are gained by performing 1000 Monte Carlo simulations to model process variation. From this diagram, it is clear that there is some margin at 800mV but there is no margin at 300mV, so SNM at 300mV is zero.

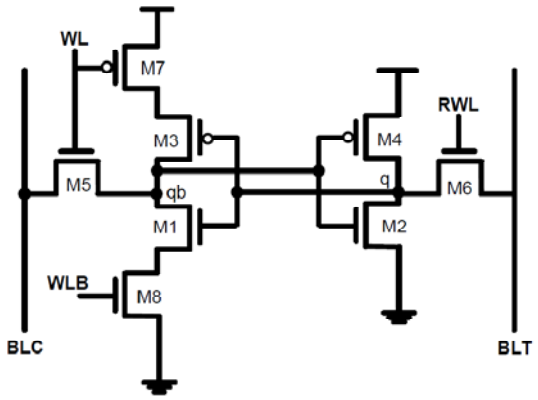
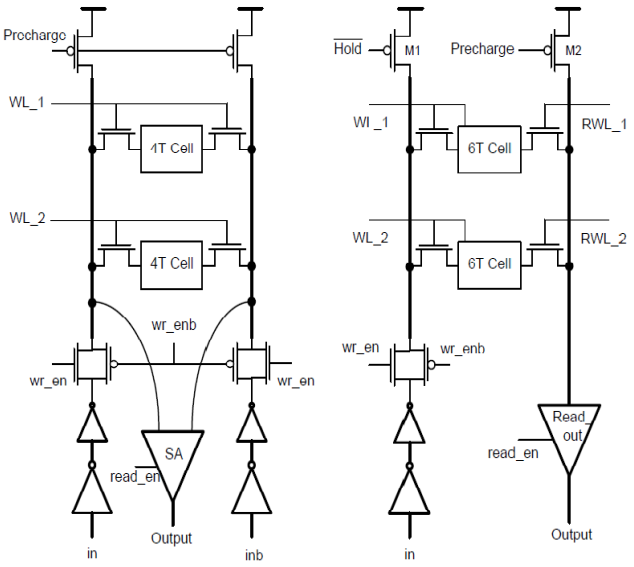


Figure 5. Proposed 8T SRAM cell for sub-threshold region.

3. Proposed 8T SRAM Cell Design

Transistor-level schematic of our proposed 8T SRAM cell is represented in figure 5 In this design read/write access transistors and their respective bit-lines are separated, to get independent read and write operations, causing a relaxation in sizing of access transistor problem. Therefore, we can choose large size write access transistor (large M5 in figure 5) to have successful write operation and a small one (M6) at read side to get successful read operation. In this proposed design, read operation is triggered by setting RWL signal to VDD, which puts read access transistor (M6) and read bit-line (BLT) in charge of performing read operation. In other side of cell, Write operation is done through M5 and BLC Bit-Line and by setting the WL to VDD. The main idea behind our improved cell is weakening the left inverter in the cell (that is figure hting with write access transistor while writing) during the write operation.

This goal is reached by adding one PMOS and one NMOS (M7 and M8 in figure 5) transistor in series with transistors of left inverter (which must be weakened during write state) in the cell. These transistors are turned off during write operation, so in the write operation supply voltage of left inverter decreases and its ground rail increases slightly. In this situation, the inverter figure hting with write access transistor is weakened and probability of successful writing will increase tremendously. To have better write operation, we can also increase the size of write access transistor slightly. At the other side, to prevent unsuccessful read operation, we can choose a minimum size transistor for read access transistor, M6.



(a) Conventional 6T SRAM (b) Proposed 8T SRAM

Figure 6. Writing and reading peripherals

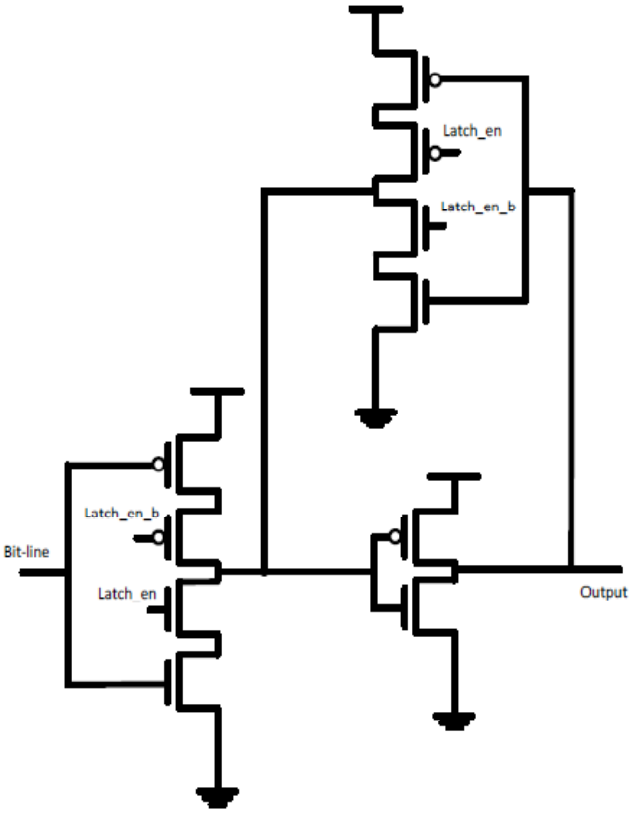


Figure 7. Read-out circuitry used in our design to accelerate reading operation

Alyet. al [9] gained an improved write-ability by adding a single transistor and using 7T SRAM. However, adding an NMOS transistor with nature of weakening the passing VDD signal is a drawback that will lead to having smaller Hold SNM that is very crucial in operation of SRAM cell.

3.1. Read and Write Operations in Proposed 8T Cell

As shown in Figure 6 (a), in conventional 6T cell, due to its differential bit-lines, read/write operations are performed differentially, so differential sense amplifiers are used to increase speed of read operation. This situation is not the same in our design. In our proposed 8T cell read and write bit-lines are separated and read/write operations are performed single ended. In other word, in our design we sacrificed the speed to get better noise margin at lower supply voltage. To be more specific, in write state the write data must be put on 'in' node (Figure 6 (b)) and in read state, content of the cell can be read from appropriate bit-line. In our design to accelerate the reading operation, a read-out circuitry similar to that of [10] was used. This read-out circuit is shown in figure 7 As depicted in figure 6 (b), in order to perform a successful writing process on cells, the write data is passed through a chain of buffers. In this chain the last inverter besides write bit-line is sized smaller to prevent unwanted increase in the bit-line capacitance.

In order to prevent this chain of buffers from impacting behavior of cells array, we used a transmission gate to cut the input data path from write bit-line when SRAM is not in write state. Therefore to control these T-gates, we used ‘wr_en’ and its complement to drive T-gate’s inputs. During write operation, the M3 (Figure 5) transistor will figureht against written 0, and M1 (Figure 5) will do the same against written ‘logic-1’ value. Consequently, in order to guarantee the superiority of access transistor, in addition to floating the VDD and GND rails of left inverter (the challenging one) and increasing size of write access transistor, size of M1 and M3 are chosen small enough. This idea also results in relaxed area overhead of adding two transistors to the cell in the proposed 8T SRAM cell. It must be noted that in conventional 6T SRAM cell to reduce the probability of unsuccessful read, size of NMOS transistors in back-to-back inverters are chosen larger than access transistors [11].

In our proposed design as shown in Figure 6 (b), to have a successful reading process, the read bit-line must be pre-charged to VDD. This operation is done using a single PMOS transistor (M2 in figure 6 (b)). So when the RWL signal is charged to VDD the content of the cell can be sensed by a single ended sense amplifier which makes the read operation even faster.

3.2. Reducing Leakage Current Between Cells and Bit-Lines

To reduce the leakage current in SRAM cell arrays, using a couple of PMOS transistors, we set the voltage of bit-lines to VDD in hold state which results in reduced leakage current between cells and bit-lines. The explanation for this behavior can be given by examining the sub-threshold current $I_{D_{sub}}$ equation shown below in Eq (1) [12]:

$$I_{D_{SUB}} = I_0 \exp\left(\frac{V_{GS} - V_T - \eta V_{DS}}{\eta V_{TH}}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_{TH}}\right)\right) \quad (1)$$

From above equation it can be deduced that, sub-threshold current depends exponentially on voltage between gate and source (V_{GS}) and if V_{GS} is reduced, sub-threshold current will decrease rapidly with a large gain. So when SRAM is in Hold mode, WL and RWL are 0, and if voltages of Bit-Lines BLC and BLT are set to VDD, then voltage between gate and source of these access transistors is equal to ‘-VDD’. Consequently, sub-threshold current is reduced exponentially. Our simulation results show that current passing through access transistor which is connected to the node that stores ‘logic-1’ is decreased but the current through access transistor neighboring the node that stores ‘logic-0’ is increased slightly. Increasing sub-threshold current for '0-stored' side is due to decreasing V_{DS} (becoming more negative) that causes the leakage current to increase according Eq (1).

Our simulation results show that setting voltage of bit-lines to VDD in hold mode decreases $I_{D_{sub}}$ for ‘1-stored’ sides by 19.41 times and increases it by 1.1 times at '0-stored' sides. The net result is that leakage current between cell and Bit-Lines is almost 10\% decreased by charging bit-lines to VDD. This method increases $I_{D_{sub}}$ at the side that stores ‘logic-0’ and decreases it at the side that stores ‘logic-1’. All cells store ‘logic-0’ at one side and ‘logic-1’ at the other side, so this method decreases the net leakage for each individual cell. Thus, the above improvement for leakage is applied for all cells in the SRAM array. In addition to decreasing leakage current, setting voltage of Bit-Lines to VDD in Hold mode will prevent these lines from floating that leads to removing the potential for undesired problems caused by floated lines.

Table 1. Sizing of transistors for conventional 6T SRAM cell

transistor	M1	M2	M3	M4	M5	M6
W/L	3.5	3.5	2	2	2.5	2.5

4. Simulation Results

We designed our proposed 8T SRAM in a 90nm industrial technology and simulated it with HSPICE 2011. The simulations were performed at 27°C, and in typical processing corner. Monte Carlo simulation is used to model the effect of fabrication process and environment variations. Table 1 shows the sizing of transistors for conventional 6T SRAM cell which we used to compare with our design.

In our proposed 8T design, $\frac{W}{L}$ for write access transistor M5 is 3, $\frac{W}{L}$ of driver transistors M1/2 are 3.5, and $\frac{W}{L}$ for other transistors are 2 (that is minimum allowable size convenient for implementation in layout). To evaluate the proposed design, we simulated the proposed 8T SRAM, conventional 6T SRAM, and three other designs reported in recently published literature. In the rest of this paper, we use WRE8T to refer to our proposed Write and Read Enhanced 8T SRAM Cell, ST10T for design of reference [13] and LP10T, and 9T for designs of [14] and [15], respectively.

Table 2. Comparison of operating metrics of our proposed 8T SRAM cell with four other designs at VDD=500mV and T=27°C

Metrics	RSNM (mV)	HSNM (mV)	Write Power. Single Cell (μW)	Leakage Power. Single Cell (nW)
WRE8T	65.9	175.4	12.48	15.08
ST10T [13]	115.9	209.9	24.46	18.69
LP10T [14]	205.6	72.2	25.18	9.33
6T conv.	72.2	178	27.31	16.32
9T [15]	178	178	26.6	16.25

Table 2 summarizes simulation results for power consumption of single write operation, leakage power for single cell, Hold SNM (HSNM) and Read SNM (RSNM) for all test cells. As mentioned earlier, WRE8T design is very low power. According to table 2, this design consumes 49% lower power compared to the previous design with lowest power consumption. This power is for a cell and its write drivers for single write operation. One of the reasons for this improvement is that in WRE8T design, write operation is single ended, so the power consumption of write drivers for this design is almost half of the others.

Lowest Leakage power for single cell belongs to LP10T design. This is due to the added tail transistor in this cell that is off in the idle mode, implying reduced leakage power due to stacking effect [16]. Although this added transistor reduces the leakage power of LP10T cell, but it makes this cell very weak during idle mode. The smallest HSNM in table 2 for LP10T cell approves this statement. After LP10T cell, WRE8T cell has the smallest leakage power due to stacking effect. At room temperature (27°C) and at VDD=500mV, leakage power of WRE8T cell is lower than conventional 6T by 15%. This improvement becomes more significant for larger VDDs and temperatures. For example, at VDD=800mV and T= 110°C, the improvement becomes 20%. ST10T suffers from high leakage power. This is due to the added two NMOS feedback transistors connected to VDD that always one of them is ON.

Simulation results that are shown in table 2 also demonstrate that HSNM and RSNM of WRE8T and 6T cell are lower than other designs and the difference between WRE8T and 6T is small. It is expected that using Fin FET transistors will improve these parameters; this part will be discussed in next section.

Figure 8 shows Write Noise Margin (WNM) of our WRE8T and other designs at three different supply voltages. As represented, WNM of the proposed cell is better than others considerably. This improvement is due to two main reasons. At the first place, the provided virtual rail in the proposed design becomes float during write operation that leads to having better write-ability. Second, due to the ability of individual sizing of access transistor in the proposed design, size of write access transistor is selected larger, which results in better write operation.

Figure 9 shows the layout of proposed 8T SRAM cell and Figure 10 shows layout of conventional 6T cell, both in an industrial 90nm technology. Dimension of WRE8T cell is 2.6μm×1.11μm while dimension of conventional 6T SRAM cell is 2.26μm×0.9μm. So the area of WRE8T cell is 29% larger than 6T. In [14], the authors compared the area of their cell and also ST10T cell with 6T. Using this information, ST10T and ST10T cells areas are 38% and 40%, respectively larger than the area of our design.

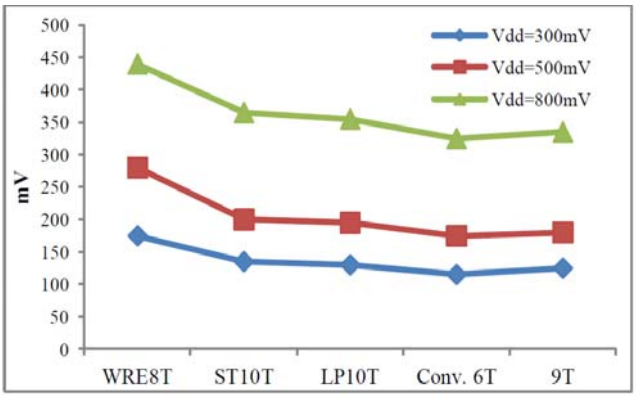


Figure 8. Write Noise Margin of different SRAM cells at three supply voltages

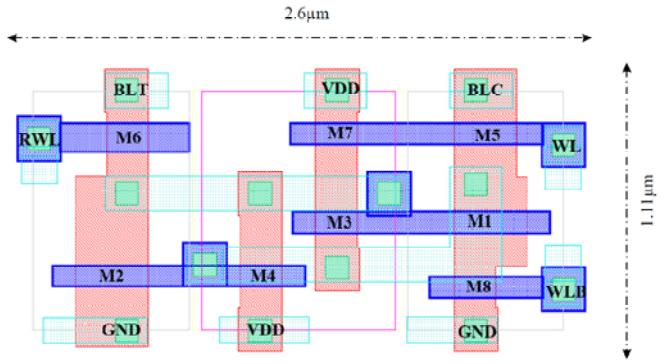


Figure 9. Layout of WRE8T cell in an industrial 90nm technology

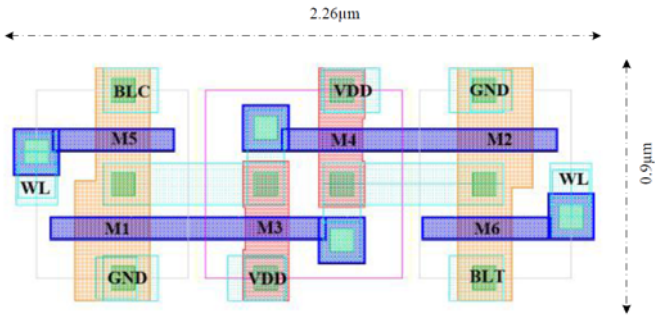
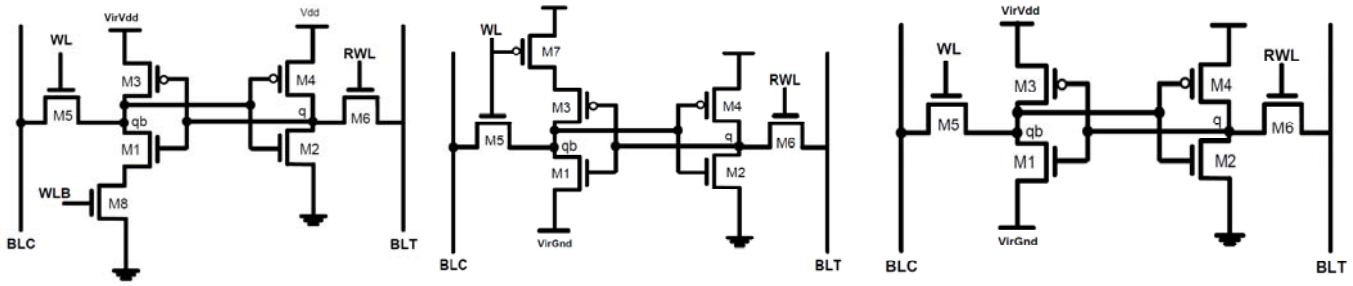


Figure 10. Layout of 6T cell in an industrial 90nm technology

5. Designing Proposed 8T Cell Using Fin FET Transistors to Improve RSNM

Fin FET transistors have sharper VTCs compared to MOSFETs. This property leads to having larger SNMs for Fin FET based SRAM cells [17].



(a) Sharing power floating rail (b) Sharing ground floating rail [8] (c) Sharing both power and ground floating rails

Figure 11. Three possible SRAM cells by sharing PMOS and NMOS transistors or both of them in WRE8T cell

Thus, to show improvement of RSNM and HSNM of proposed 8T SRAM cell and to test the scalability of the design, we designed this cell using 16nm PTM technology [18] using both Fin FET and Bulk-CMOS transistors. Due to better control on the channel in Fin FET transistors, these transistors exhibit better leakage power, larger I_{on}/I_{off}, and larger subthreshold slope factor compared to MOSFETS [19]. Thus, in this section we are not worry about degrading this metrics using Fin FET transistors and just extracte and compare SNMs. Table 3 lists RSNM and HSNM of proposed 8T SRAM cell using Fin FET and Bulk-CMOS transistors. As seen, Fin FET based SRAM cell improves both RSNM and HSNM considerably.

By comparing HSNM for Fin FET based SRAM for proposed cell with HSNM of the best design in table 2, it can be understood that by designing our proposed cell using Fin FET, HSNM of our design will reach to the design with the best HSNM in table 2.

6. Integration of Proposed Cell in the SRAM Array

In the proposed 8T SRAM cell, a PMOS and an NMOS transistor is added to the cell. These transistors provide virtual power and ground rails in write operation to improve write-ability of the cell. These transistors can be shared between some neighboring cells in the SRAM array. Depending on that which of these NMOS or PMOS transistors are shared, three possible SRAM cells might exist. Figure 11 shows these three possible SRAM cells. 7T SRAM cell in Figure 11 (b) was used in our previous work [8]. In this paper to further reduce the number of transistors in each SRAM cell, we used the third architecture (Figure 11 (c)).

In these new SRAM arrays, there are some possible architectures to share floating power and ground rails. Figure 12 shows three possible architectures for sharing virtual rails. In this figure, in part (a) virtual rails are shared among all cells in the array and in part (b) these rails are shared for all cells in the same column. In these architectures, there are some cells that power and ground rails of them are floated while they are not selected (their word-lines are set to 0). These cells are called 'half selected (HS)' cells. Half selected cells have potential of un-stability and in this figure are shown by light brown color. Simulations show that when using SRAM cells of figures 11 (a), 11 (b), and 11 (c), mean of hold SNM in 1000 runs of Monte Carlo simulations for half selected cells are 0.55mV, 32.15mV, and 5.28mV, respectively at supply voltage of 500mV.

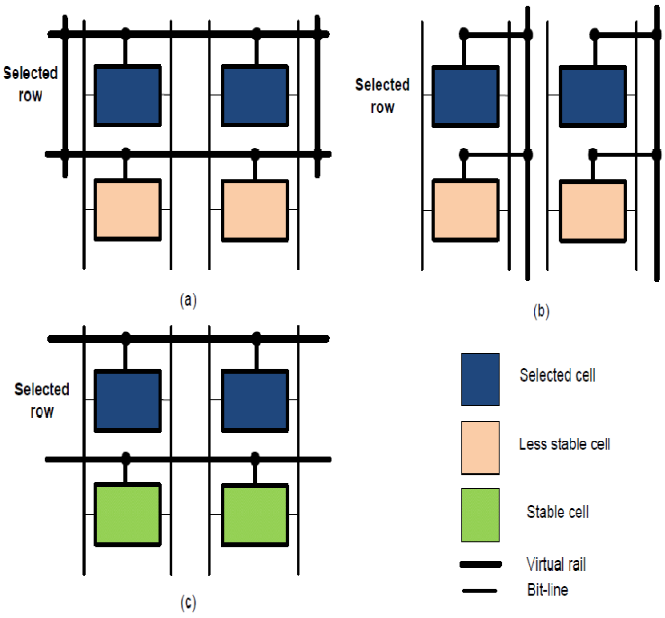


Figure 12. Three possible architectures for sharing power and ground rails: (a) sharing virtual rails for all cells in the array; (b) sharing virtual rails for each column; (c) sharing virtual rails for each row

Table 3. RSNM and HSNM comparison for proposed 8T SRAM cell using Fin FET and Bulk-CMOS transistors

Design	RSNM (mV)	HSNM (mV)
Fin FET based cell	93.5	202.5
Bulk-CMOS based cell	10	134.9

Table 4. Power consumption comparison for two cases in architecture of figure 14

VDD=1.0V	Case 1*	Case 2^o	WRE8T
Write power (μW)	68.34	9.87	9.83

*In this case voltage of right internal node in SRAM cells of the same column are set to '1'.
^{o}In this case voltage of right internal node in SRAM cells of the same column are set to '0'.

These SNMs are not acceptable at supply voltage of 500mV and even thermal noise at room temperature (kT=25mV) can flip the content of the cell. Therefore, the half selected cells in architectures of parts (a) and (b) in Fig. 12 are susceptible to losing their data. Fig. 13 shows distribution of hold SNM for WRE8T cell at 500mV. Average of this distribution is 168.93mV. This value is large enough for the cell to retain its data at normal conditions.

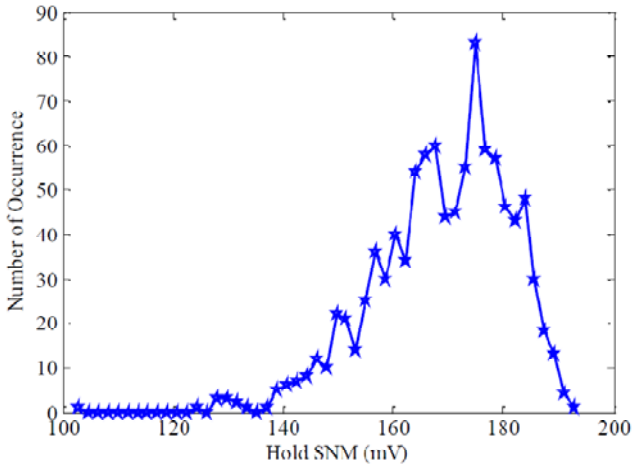


Figure 13. Distribution of hold SNM of WRE8T SRAM cell at supplyvoltage of 500mV

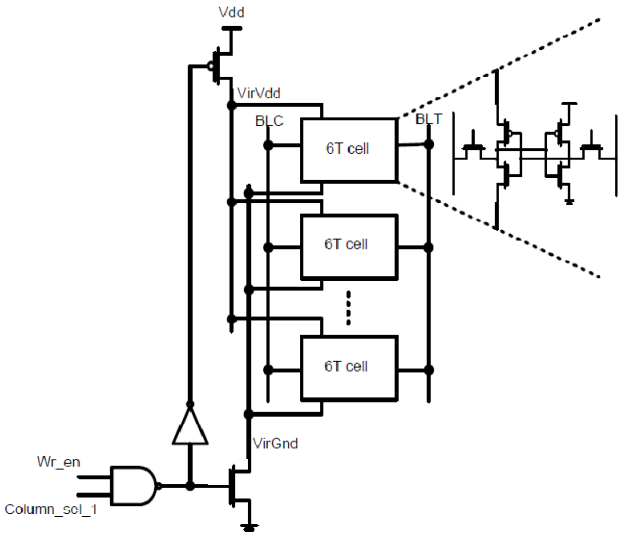


Figure 14. Distribution of virtual power and ground rails in case that both of these floating rails are shared between cells in the same column

Authors in [20] distributed virtual rails such as Figure 12 (a). If we use this architecture in our design, architecture of one column in the SRAM array can be such as figure 14 In this architecture, added NAND gate and the inverter will turn the PMOS and NMOS transistors of floating rails off, only in write operation, as desired. This design faces a serious problem. Consider that voltage of left internal nodes in all cells sharing a column is '0', so left NMOS driver transistor in all of these cells will be on. Now in write operation's duration, to write '1' in the left nodes of top cell in the column (qb1 in figure 15), some currents will pass through the NMOS driver transistors of bellow cells and increase the voltage of internal nodes of these un-selected cells. So, this sneaky current will increase the activity of nodes and thus, increasing the write power.

To test the effect of this sneaky current on power consumption, a column of SRAM such as figure 14 was designed and besides a selected cell, 64 other unselected cells (their WL are set to 0) were put in the column. At first case, voltage of right internal nodes in all cells are set to 'VDD' so that the NMOS driver transistors become on and the strategy for sneaky current becomes available. At the second case, the voltage of right internal nodes in the unselected cells were put to '0', so that the sneaky current cannot pass from PMOS transistor of write driver to the left internal nodes in unselected cells. As depicted in table 4, simulations at VDD=1.0V and Temp=27^{o}C show that, due to existence of sneaky current in case 1, write power is 6.92 times larger than case 2 that there is no sneaky current. Thus, the sneaky current will increase the total power consumption considerably. In table 4 write power of proposed 8T cell is shown, too. The sneaky current is shown in figure 15.

In this figure the left inverters of the cells sharing same column are shown and the path of sneaky current in one state of stored data in the cells are demonstrated. Besides degradation of power consumption, this sneaky current can degrade SNM and reliability of the SRAM cells and if its duration and value become large enough, it can flip the content of the half selected cells.

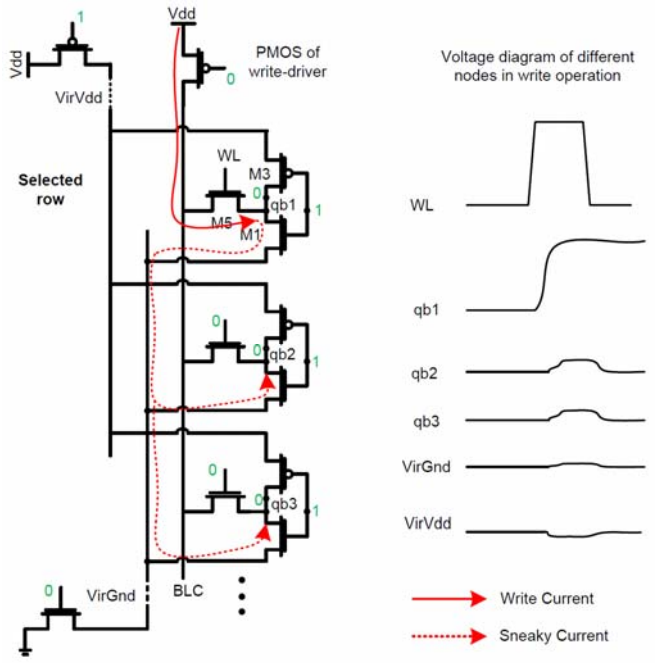


Figure 15. Sneaky current in architecture of figure 14 that can change voltage of internal nodes in half selected cells

Due to above discussion, using architectures of figure 12 (a) and b are not suitable choices for integration of SRAM cells. In architecture of figure 12 (c), there are no half selected cells. In other words, power and ground rails of just selected cells become virtual. Thus, problem of potentially unstable cells is removed. Also in this architecture, discussed sneaky current, that exists in write operation for architectures of (a) and (b) (Figure 12) is removed. Therefore, this architecture is suitable for implementing our proposed

SRAM. In this architecture also shared floating power and ground rails of left inverter in the cells can be obtained with neighboring cells in the same row.

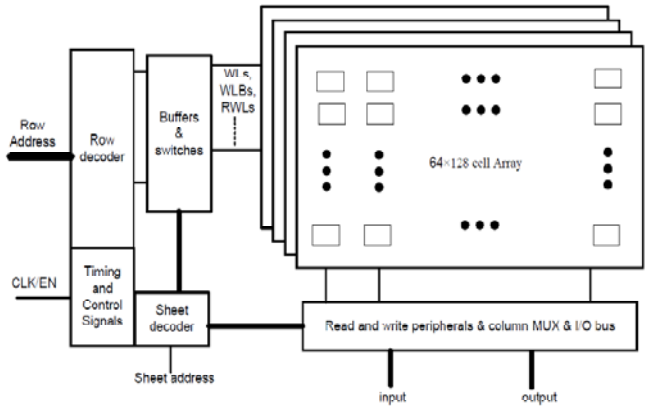


Figure 16. Micro architecture of 32kb SRAM

Table 5. Operating Parameters at VDD=800mV for 32kb SRAMUsing Proposed Design

Read Power	519 μW
Read Energy	0.36 pJ
Write Power	857μW
Write Energy	7.5 pJ
Operating Frequency	1.43 GHz

In the selected architecture, it is important to choose proper sizes for NMOS and PMOS shared transistors responsible for creating floating rails. Also the optimum number of cells that can share the floating rails should be determined. In [21], authors used the same architecture for integrating cells. The difference between this architecture and our design is that in [21], only floating rail for ground was considered, whereas we distribute floating rails for both ground and power. In [21] a good discussion on optimizing the number of cells in a row sharing floating ground rail (N) and also determining the size ($\beta.N.W_{min}$; where $\beta$is ratio of width of NMOS VSS-switch transistor and NMOS driver transistor in the SRAM cell, and W_{min} is the minimum allowed size for width of a transistor in technology) of NMOS transistor responsible for creating floating rail were drawn. Using similar procedure, we choose N=4, and β=3 for our design.

Finally, a 32kb SRAM using proposed scheme was designed in 90nm industrial CMOS technology. Figure 16 shows the micro architecture of designed SRAM. In this SRAM, four arrays of 8kb cells were considered and a 2-to-4 sheet decoder was used for selecting the proper sheet. Table 5 shows power, energy, and operating frequency (inverse of cycle time) at supply voltage of 800mV. Cycle time is the time between activation of address decoders, until 50mV voltage difference occurs between read bit-lines [14].

7. Conclusion

A new tri-state based SRAM cells is presented. In this design, by adding one PMOS and one NMOS transistor that become OFF during write operation, feedback loop in the cell becomes weaker, hence write-ability is improved considerably. At first, these added NMOS and PMOS transistors are considered for each cell individually that leads to eight transistor (8T) design for SRAM cell. Proposed 8T SRAM cell, conventional 6T cell, and three other cells from the recent literature are designed in a 90nm industrial technology. Simulation results show that proposed 8T SRAM cell, consumes 54% lower power than conventional 6T SRAM for single write operation at supply voltage of 500mV and 20% lower leakage power at VDD=500mV and Temp=110^{o}C. Finally, a 32kb SRAM based on proposed design is implemented that consumes 0.36pJ and 7.5pJ energy for single read and write operations, respectively. In this SRAM, PMOS and NMOS transistors which are responsible for creating floating power and ground rails are shared among four cells in the same row leading to an equivalent 6.5T SRAM cell.

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Paper Handling Data:

Submitted: 14.05.2014
Received in revised form: 15.10.2014
Accepted: 20.10.2014
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