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An Ultra-Efficient Imprecise Adder for Approximate Computing Based on CNTFET

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Abstract

Nowadays, mobile multimedia consumer electronic devices are wildly used. These battery-dependent and energy constraint devices require very low power consumption. However, as they are associated with human senses, they can perform complex arithmetic operations with a degree of impreciseness, which is not sensed by a human. In this paper, an ultra-efficient imprecise serial adder is proposed for approximate computing based on carbon nanotube FETs (CNTFETs). Serial addition is suitable for low-energy applications and leads to a considerable design efficiency. It is also well known that the CNTFET device can be a feasible replacement for the CMOS technology. In this design the resemblance of Carry' and Sum and a simple Cout' generator are utilized to provide an imprecise adder. The circuits are simulated using HSPICE with the Stanford CNTFET model at 32 nm feature size. The results indicate that the proposed method leads to considerable improvement in terms of performance and power consumption, while having fewer devices and small power-NED product.

Keywords: Approximate Computing, Low-Power, Serial Adder, Carbon Nanotube Field Effect Transistor (CNTFET), Nanoelectronics.

1. Introduction

By extensively wide use of portable consumer electronic devices and serious battery constraints, low-power design has become much more of demand. Low-power design methods at different levels of abstraction has been successfully utilized to minimize the power consumption.

Computational functions of the recent digital systems extensively involve of applications that includes audio, video and image processing. In addition, the restricted cognitive capability of humans in detecting an image or a video allows the outputs of media processing algorithms not to be numerically accurate. Accordingly, approximate computation becomes admissible by the laxity on numerical accuracy due to this human restriction. The imprecise complex arithmetic functions require drastically simpler hardware which leads to considerable saves in energy consumption and area. Accordingly, imprecise computing can be considered as one of the most effective low-power design methods in many digital signal processors [1-3]. Adders are the most important and fundamental block in digital signal processors and improving the performance metrics of this cell can improve the performance metrics of the whole processor.

Various imprecise full adder cells based on different logic styles have been presented so far in the literature [2, 3]. Most of these imprecise full adders have been designed by means of reduction of the conventional CMOS mirror and hybrid pass transistor- based full adders [4] and according to the number of states that Sum and C_{out} signals are equal. It is worth mentioning that in these imprecise full adders by more reducing the number of transistors the number of erroneous outputs increases. Increasing the number of errors in C_{out}

signal can lead to error propagation throughout the n-bit ripple carry adders. In addition, errors in Sum signal can be propagate throughout the adders with tree structure.

On the other hand, by scaling down the technology in nanometer dimensions conventional CMOS technology has encountered serious limitations and challenges, such as short channel effects, reduced gate control, very high leakage currents, very high power density and reliability issues [5]. Many nanoscale devices have been introduced so far to resolve these problems for the near future energy-efficient applications. However, among these nanotechnologies, carbon nanotube FET (CNTFET) seems to be the most feasible alternative due to its extraordinary electrical properties as well as its higher resemblance with MOSFET [6-8]. CNTFET benefits from near ballistic carrier transport, lower leakage currents, smaller parasitics and same mobilities for electrons and holes. In addition, the desired threshold voltage for a CNTFET can be achieved by determining the diameter of the CNTs under the gate.

According to the above discussions designing an efficient imprecise adder cell based on carbon nanotube FETs is highly of demand. In this paper an ultra-efficient CNTFET-based imprecise serial adder cell is proposed for energy-efficient nanoelectronic-based approximate digital signal processors.

In the remainder of this paper, in Section 2 the proposed design is introduced. Simulation results and comparisons are given in Section 3. Finally Section 4 concludes the paper.

2. Backgrounds

2.1. Carbon Nanotube FET (CNTFET)

In CNTFET, intrinsic semiconductor carbon nanotubes (CNTs) are utilized as the channel of the transistor. In addition, highly doped semiconductor CNT regions are utilized as the source/drain regions of the transistor. The conductivity of the channel CNTs are electrostatically controlled by a metal gate via a high-k gate insulator. CNTFET benefits from near ballistic carrier transport, lower leakage currents, smaller parasitics and same mobilities for electrons and holes. Moreover, the mobility of electrons and holes are the same in CNT. A great feature of CNTFET is that the desired threshold voltage can be achieved by determining the diameter of the CNTs under the gate according to Eq. 1 [5].

$$V_{th} = \frac{0.436}{D_{CNT}(nm)} \tag{1}$$

It is evident form Eq. 1 that the threshold voltage is inversely proportional to the diameter of CNTs. The diameter of a CNT is calculated based on its chirality indices (n_1, n_2) as given by Eq. 2 [5].

$$D_{CNT} = 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{2}$$

It is worth mentioning that many effective and feasible solutions have already been presented in the literature for growing CNTs with a specific diameter and CNTFETs with a desirable threshold voltage [9, 10].

2.2. Imprecise Full Adder Design

Many widely used applications such as audio, video and image processing that involves human sensesdo not requirenumerically accurate media processing algorithms. The inexact complex arithmetic operations require quite simpler hardware which leads to considerable area and energy efficiency. Accordingly, inexact computing is one of the most effective methods for designing many efficient digital signal processors [1].

Besides lower power consumption and transistor count, some critical precision evaluation metrics including Mean Error Distance (MED) and Normalized Error Distance (NED) [11] are utilized to evaluate the preciseness of the approximate designs. In general, error distance (ED) is defined as the arithmetic distance between an erroneous output generated by an imprecise circuit and its exact value. Accordingly, the mean value of the EDs of all possible outputs for a circuit is indicated as Mean Error Distance. It is notable that MED is useful in evaluating the efficiency of an inexact design and normalized MED which is indicated as NED is used in characterizing the reliability of an inexact design. These preciseness parameters can be calculated according to Eqs. 3 and 4.

$$MED = \sum_i ED_i * p_i \tag{3}$$

$$NED = \frac{MED}{D} \tag{4}$$

where p_i is the probability of accruing i^{th} input, and D is the maximum amount of error that an imprecise adder can have. It is worth mentioning that the power-NED product is usually calculated to make a trade off between power and precision of approximate designs.

Many imprecise full adders have already been presented in the literature. The first imprecise FA presented in [2] is an imprecise design of the mirror CMOS full adder which is shown in figure 1. It is evident that, this design has eight fewer transistors than the exact mirror full adder cell. In this design, one error exists in the C_{out} output and two errors exist in the SUM output.

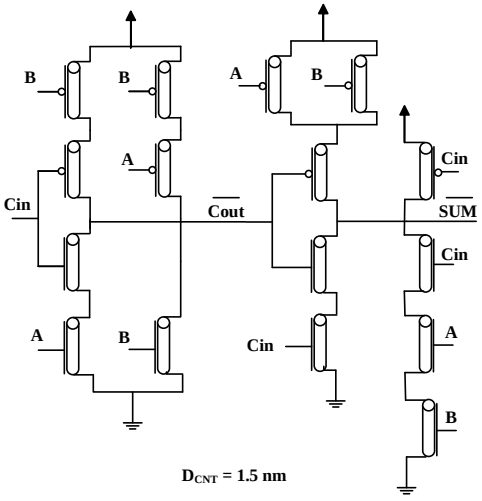

Figure 1. The first imprecise full adder of [2]

The second imprecise full adder of [2] is illustrated in

figure 2. In the design of this adder cell the fact that the SUM output is negate of the C_{out} output in six input combinations out of total eight combinations. In this design the C_{out} output is completely exact while the SUM output has two errors.

The third full adder presented in [2] is a combination of the first and the second described full adders which is shown in figure 3. This design reduces the transistor count more than the previous two cells and has three errors in the SUM output and one error in the C_{out} output.

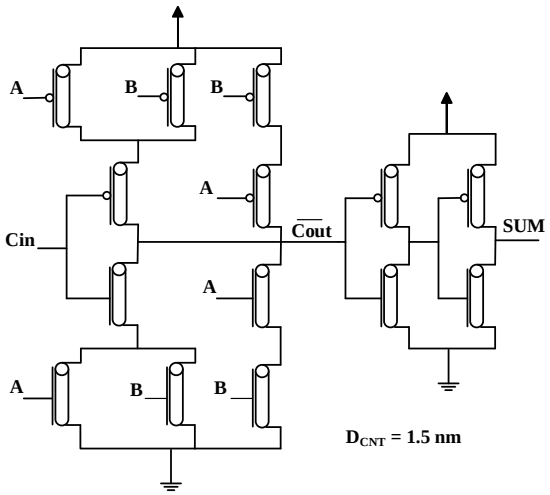

Figure 2. The second imprecise full adder of [2]

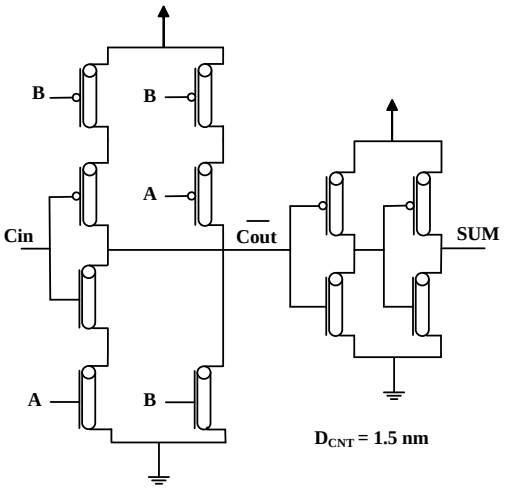

Figure 3. The first imprecise full adder of [2]

It can be derived from the truth table of the full adder circuit that the C_{out} output is similar to the A and B inputs for six input combinations. Based on the interchange relation between A and B inputs, the C_{out} output is deliberated from the A input in the fourth inexact full adder of [2]. In this full adder demonstrated in figure 4, an inverter generatesthe C_{out}' from the input A and a module generates SUM from Cout' similar to the first dull adder. This inexact full adder has three errors in SUM and two errors in C_{out}.

The first imprecise full adder of [3], which is shown in figure 5, is designed based on the pass transistor logic style. As the SUM signal of an accurate full adder is equal to C_{in} in half of the input combinations, the inexact SUM is considered equal to C_{in} in this imprecise full adder. In addition the Cout signal is calculated according to Eq. 5. In this imprecise full adder, both C_{out} and SUM signals are exact for the half of input combinations.

$$C_{out} = \overline{(A \oplus B)C_{in} + \bar{A}\bar{B}} \quad (5)$$

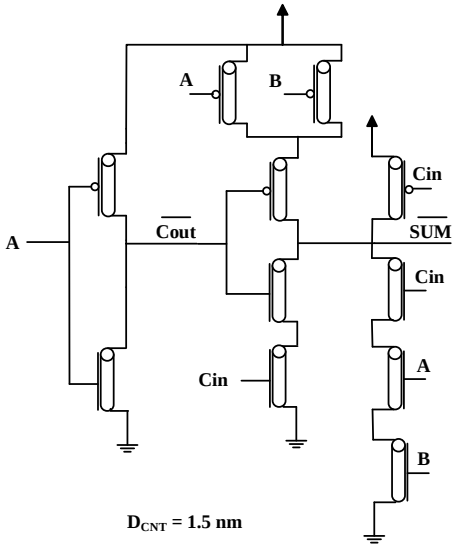

Figure 4. The fourth imprecise full adder of [2]

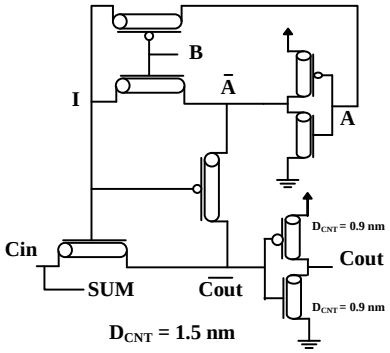

Figure 5. The first imprecise full adder of [3]

The second imprecise full adder of [3], which is depicted in figure 6, has six transistors and is designed based on pass transistors. In this circuit the SUM signal is equal to XNOR of A and B and the Cout signal is calculated according to Eq. 6. In this cell the SUM signal is correct in four input combinations and the C_{out} signal is totally accurate.

$$C_{out} = (A \oplus B)C_{in} + AB \quad (6)$$

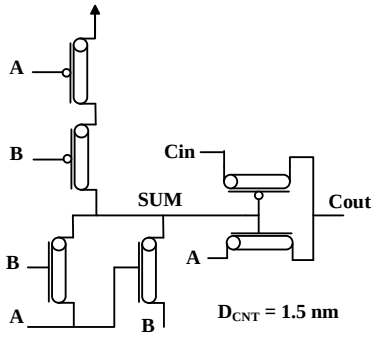

Figure 6. The second imprecise full adder of [3]

The third inexact full adder of [3], shown in figure 7, is an extension of the previously discussed imprecise design. In

this XNOR-based full adder, two additional pass transistors are utilized to enhance the preciseness of the SUM signal. In this circuit, SUM has two errors and the C_{out}output is accurate for all the possible combinations. The functionality of this inexact cell is given in Eqs. 6 and 7.

$$SUM = \overline{(A \oplus B)} C_{in} \tag{7}$$

$$C_{out} = (A \oplus B) C_{in} + AB \tag{8}$$

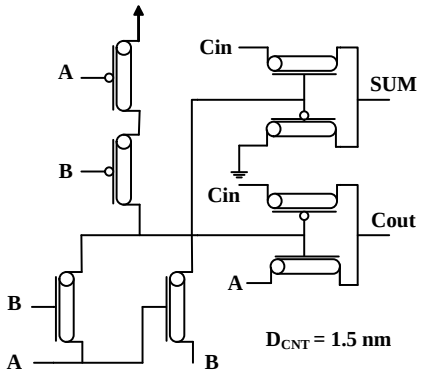

Figure 7. The third imprecise full adder of [3]

3. The Suggested Imprecise Adder

The core of an imprecise serial adder is an approximate full adder cell. The suggested imprecise full adder cell for this design is indeed an efficient three-input minority circuit [12], which is shown in figure 8. The conventional mythologies for implementing minority function leads to a higher number of transistors and consequentlyhigher power, longer delay and energy consumption overhead. The minority function can be implemented using a capacitive voltage division followed by an inverter with a switching threshold of '0.5' logical value [12]. The Voltage Transfer Characteristic (VTC) of the utilized inverter is given in figure 9. It indicates that the inverter has a '0.5' logical switching threshold. It is worth pointing out that CNTFET-based inverter has a quite sharper curve in the transition region due to the considerably higher gain, which significantly improves the noise margins [13]. The determinable switching threshold and a considerably high inherent voltage gain of the CNTFET inverter makes it very suitable for implementing minority function.

In a three-input minority gate, shown in figure 8, four different voltage levels including 0V, $V_{DD}/3$, $2V_{DD}/3$ and V_{DD} are generated by the capacitive voltage divider. When all inputs are low or only one of the inputs is high and consequently the voltage at the gate of the inverter is 0V or 0.3V, respectively, according to the VTC of the inverter, the output of the minority gate is high (0.9V). When all inputs are high or only one of the inputs is low and consequently the voltage at the gate of the inverter is V_{DD} or 0.6V, respectively, according to the VTC of the inverter, the output of the minority gate is low (0V). The transient response of the inexact full adder is shown in figure 10, which indicates its correct functionality and proper operation.

It is worth mentioning that the inner node C_{out}* of the propose design has lower noise margin ($V_{DD}/6$) than usual as it has voltage levels of $V_{DD}/3$ and $2V_{DD}/3$ in addition to 0V and V_{DD}. However, it should be taken into account that the main sources of noise injection are the circuit inputs and the noise margin in these nodes are $V_{DD}/2$ for the proposed design. This is because a $V_{DD}/2$ change at the input voltage is required to change the C_{out}* node by $V_{DD}/6$.In addition, it is worth mentioning that the proposed full adder is more efficient than its counterparts that some of them have the threshold drop problem in their inner nodes. Moreover, the imprecise full adders are utilized in approximate applications where noise is more tolerable than the normal applications.

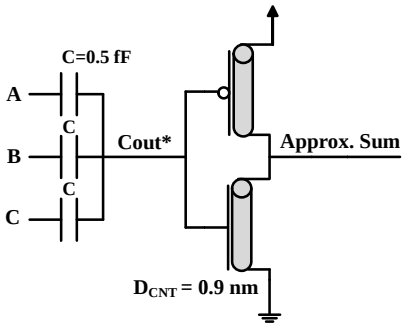

Figure 8. The utilized imprecise FA based on [12]

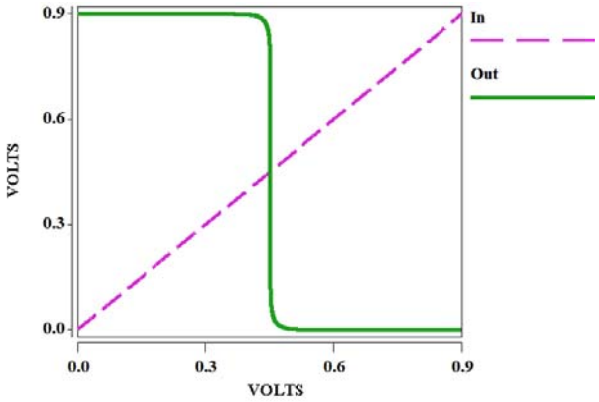

Figure 9. DC analysis of the CNTFET Inverter (D_{CNT}=0.9 nm)

As the minority function and the Sum signals are the same except for '000' and '111' inputs, in the suggested imprecise full adder minority is used as the Sum signal [2]. In addition, the input of the inverter, denoted as C_{out}*, is logically the same as C_{out} of an exact full adder, but with an incomplete voltage swing when the inputs are not '000' or '111'. However, it is notable that this incomplete voltage swing (but with a correct logic) will become rail-to-rail when it reaches to the gate of the next stage. In addition, in some applications such as serial adder, the inner inverter in the circuit can be utilized to generate the full-swing C_{out} signal without any redundancy to the original imprecise full adder.

It is notable that the discussed approximate full adder cell can be effectively used in imprecise serial addition and considerably reduces the hardware overhead. It is worth mentioning that serial addition is suitable for ultra-low-energy applications and leads to a significant design efficiency [14]. The proposed approximate serial addercircuit is illustrated in figure 11. As shown in figure 11, the adder part of the serial adder is reduced to just a capacitor network and the required invertings are embedded in the D-flip flop. In fact, one of the inverters of the D-flip flop is utilized for

two purposes; generating the approximate SUM signal and implementing the master latch of the flip flop. The transient response of the proposed approximate serial adder is shown in figure 12, which authenticate its correct operation.

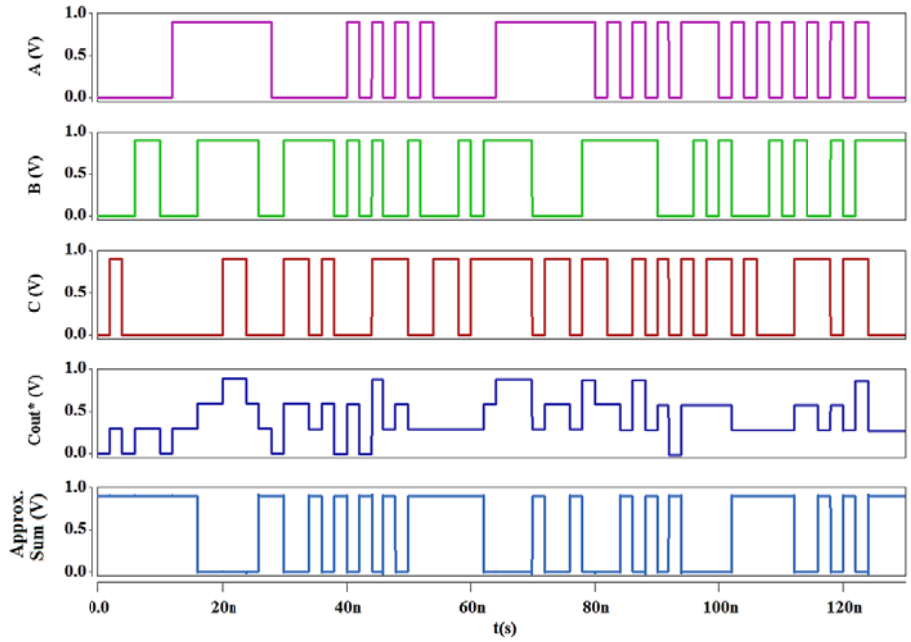

Figure 10. The transient response of the imprecise full adder cell

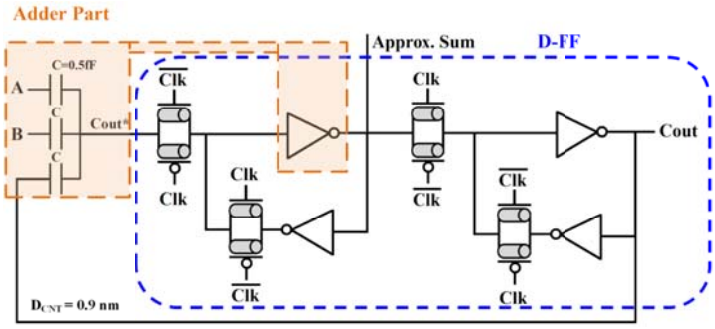

Figure 11. The proposed approximate serial adder

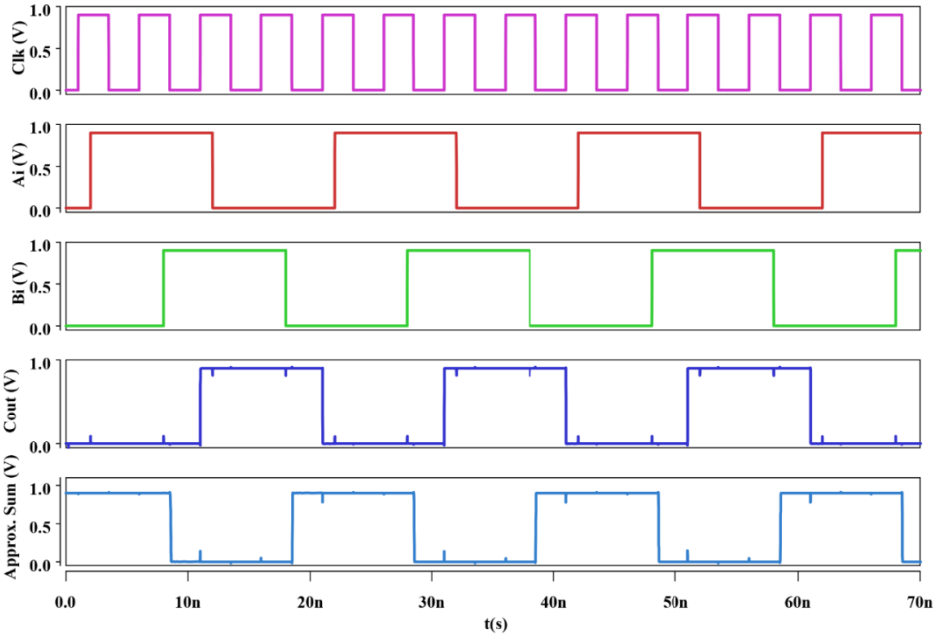

Figure 12. The transient response of the proposed approximate serial adder

4. Simulation Results and Comparison

The imprecise adders are compared in terms of delay, power consumption, energy-efficiency, error metrics and design complexity in this section. The HSPICE simulations are conducted using the Stanford SPICE model for 32nm CNTFE [15, 16] considering all the transitions for different input combinations to evaluate correct delay and power metrics.

The simulation results of the inexact full adders are given in table 1 According to the result the suggested full adder has considerably lower propagation delay, average power and energy consumption as compared to the other state-of-the-art inexact full adders implemented and optimized for 32 nm CNTFET technology. This is due to the lower number of devices, simpler structure and short critical path of this design. In addition, in terms of reliability, the suggested design as well as three other designs have the minimum total error distance. However, the suggested inexact full adder cell has considerably lower power-NED product that specifies the efficacy of a design in trading off preciseness for power.

Furthermore, table 2 presents the characteristics of the approximate serial adders. The results indicates that the proposed imprecise serial adder has lower power consumption due to its simpler structure.

5. Conclusion

Portables multimedia consumer electronic devices are commonly used. These energy constraint devices demand very low power consumption. However, as they are associated with human senses, the can carry out complex arithmetic operations with a degree of impreciseness, which is not sensed by a human. In this paper an efficient inexact serial adder has been presented for imprecise computing based on carbon nanotube FETs (CNTFETs). The CNTFET device is known as the most feasible replacement for the CMOS technology. In the proposed design similarity of Carry' and Sum signals in ¾ of input combination and a simple C_{out}' generator module are utilized to reach efficient imprecise adder. The circuits are simulated using HSPICE with the Stanford CNTFET model at 32 nm technology node. The results indicate that the proposed method leads to considerable improvement in terms of design complexity and power consumption.

Table 1. Approximate full adders results

Designs	Power (nW)	Delay (ps)	Energy (aJ)	TED	NED	NED × Power
1st design of [2]	27.578	17.210	0.475	2	0.083	2.289
2nd design of [2]	35.277	14.586	0.515	2	0.083	2.928
3rd design of [2]	32.400	13.452	0.436	3	0.125	4.050
4th design of [2]	25.510	15.166	0.387	3	0.125	3.189
1st design of [3]	216.04	80.402	17.37	4	0.166	35.86
2nd design of [3]	20.397	30.329	0.619	4	0.166	3.386
3rd design of [3]	26.619	76.158	2.027	2	0.083	2.209
Suggested	**6.1513**	**10.056**	**0.062**	**2**	**0.083**	**0.511**

Table 2. Approximate serial adders results

Imprecise full adder cells	Average Power (nW)	Number of Devices
1st design of [2]	64.254	34
2nd design of [2]	57.045	30
3rd design of [2]	54.678	25
4th design of [2]	63.340	31
1st design of [3]	259.82	24
2nd design of [3]	53.055	22
3rd design of [3]	65.480	24
Proposed design	**48.544**	**19**

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