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A Low-Power Hierarchical FinFET-Based SRAM

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Abstract

In this paper, a low-power energy-efficient hierarchical SRAM design capable of working in near-threshold region is proposed. The proposed method enhances the noise margin using an extra circuitry, while restricting the hardware redundancy by sharing the additional circuitry between each two SRAM cells in a hierarchical style. The results of simulating the FinFET-based SRAM cells using Synopsys HSPICE at 10nm technology node indicate that the proposed design reduces, on average, the power-delay product, read and write delays by 14.34%, 2.37% and 8.54%, respectively, and significantly improves the static noise margins even in the presence of major process variations.

Keywords: Static Random Access Memory (SRAM), Multiport Memories, Low-Power Design, Static Noise Margin (SNM), FinFET, Nanoelectronics.

1. Introduction

Nowadays, by scaling the technology node, the variability concerns have become very important. This is due to (i) very small geometrics where even small variations can cause big changes, (ii) reduced power supply voltage, where V_{DD} level is very close to transistors threshold voltage [1]. Accordingly, the SRAM cell stability depending on transistors strength ratios has become one of the biggest concerns in VLSI design [2]. With the ever-increasing short channel effects, parametric variations and cache capacity, SRAMs have become very sensitive to variability. As a result, a new trade-off between the variability, power consumption and performance parameters has come in VLSI design [2].

Ignoring redundancy, each cell must work under worst-case variations. In the conventional 6T SRAM, strength ratios of devices must be adopted such that cell static noise margin and write margin are both upheld, while they are in conflict with each other. During the read state, it is desirable to have stronger storage inverters and weaker pass transistors, while during the write state it is desirable to have stronger access transistors and weaker storage inverters. This fine balance of transistor strength ratios can be easily affected by process variations, which will specifically degrade cell stability and read margin in nanoscale technologies [2].

In order to consider variability problems, many design techniques have been proposed to enable low-voltage operation for SRAM cells. A higher supply voltage can be used for SRAM cells such that the SRAM voltage does not decrease with the technology to meet the desirable margins [3]. However, this approach does not provide the demanded low power consumption. Another approach is to use dynamic voltage sources such that SRAM voltage source can dynamically change during different states [4]-[5]. This technique increases the design complexity, while it improves the cell stability and reduces the standby leakage.

Scaling the technology node has also led to a major power consumption challenge. The importance of power consumptions is more prominent in the systems with restricted energy sources. Reducing the supply voltage is considered as one of the most effective ways to decrease the power dissipation. This is achieved by sub-threshold or near threshold circuits design which enhances energy efficiency [6]. In this way, leakage power is also considerably reduced due to less voltage difference between drain and source of a transistor, which suppresses the DIBL effect, and consequently reduces the OFF current [7].

On the other hand, reducing the supply voltage results in higher propagation delay and slower circuits. At the present time, power saving is becoming very crucial in many circuits and applications that do not require very high speed, such as memories, nano-sensors, radio frequency identification and implantable medical devices. These applications may be in hold or stand-by modes most of the time, and need very low energy consumption and long battery lifetimes [8]. In addition, investigations have demonstrated that the minimum energy can be achieved in the sub-threshold region. In other words, appropriate power-delay product (PDP) can be found in the near-threshold region [9]. In the sub-threshold region, the drain current is defined by Eq. 1 [10].

$$I_{sub} = \mu c_{ox} \frac{W}{L} e^{1.8} \phi_T^2 \, e^{\frac{V_{GS}-V_{th}}{n\phi_T}} \left(1 - e^{\frac{-V_{DS}}{\phi_T}}\right) \quad (1)$$

where, $n = 1 + \frac{C_{dep}}{C_{ox}}$ is the sub-threshold factor and $\emptyset_T$is the thermal voltage.

A specific and important state of a transistor in a nanoscale digital circuit is the OFF state, where V_{GS}=0V and V_{DS}=V_{DD}. The drain current in this state, which is denoted as I_{OFF}, is given by Eq. 2. It can be concluded from Eq. 3 that the I_{OFF} leakage current is reduced exponentially by decreasing the supply voltage.

$$I_{OFF} \simeq \mu c_{ox} \frac{W}{L} e^{1.8} \phi_T^2 \, e^{\frac{-V_{th}}{n\phi_T}} \quad (2)$$

On the other hand, reducing the supply voltage to near-threshold region considerably increases the circuit delay. The propagation delay in the sub-threshold region is almost given by Eq. 3, where K is a suitable fitting coefficient.

$$t_d \simeq \frac{KCV_{DD}}{\mu c_{ox} \frac{W}{L} e^{1.8} \phi_T^2 \, e^{(V_{GS}-V_{th})/n\phi_T}} \quad (3)$$

Due to a significant speed reduction, sub-threshold circuits are often unsuitable for high-performance applications. However, they are practical for some applications, which do not require high-frequency operation but demand ultra-low power consumption, such as wireless sensor networks. However, increase in variations in sub-threshold region can degrade circuit stability [17].

SRAMs occupy a considerable part of the area and dissipate a large amount of power in VLSI chips [16]. Therefore, reducing the power consumption in SRAM cells is a vital issue in low-power VLSI design. As SRAM cells are often in the hold state, decreasing the static power dissipation of SRAM cells considerably contributes in reducing the total power consumption of a chip. Operating of SRAM in the sub-threshold region can dramatically reduce the leakage power, but it degrades the speed and static noise margin (SNM) of the cell, which should be considered in the design methodology [8].

In order to meet the challenges imposed by transistor scaling, different device structures have been explored as alternatives to the conventional bulk MOSFET. However, considering these technologies, FinFET is more appropriate for scaling the MOSFET to near 10nm feature size [11]. FinFETs demonstrate superior gate control on the channel, lower sub-threshold swing, lower short channel effect and higher scalability. However, width quantization is a challenge in FinFETs, which restricts the design possibilities of FinFET-based circuits such as SRAMs that need transistor sizing for correct operation and robustness. This constraint should be carefully considered and compensated in the design procedure [12].

In this paper, a new hierarchical SRAM cell design, denoted as HSRAM, is proposed with improved SNM and static and dynamic power consumption metrics. The number of transistors in every cell is decreased compared to its counterpart presented in [14], by multiplexing the additional transistors between each two cells, which reduces the power and energy consumptions of the proposed design.

The rest of this paper is organized as follows: In the next Section related work is reviewed. The proposed SRAM cells are introduced and described in the Proposed Design Section. The simulation results and comparisons are given in Simulation Result Section, and finally Summery Section concludes the paper.

2. Related Work

Designing low-voltage memories is demanded to reach lower power consumption. The classic 6T (6-transistor) SRAM cell is shown in figure 1. Assume that the X and Y nodes have stored 0 and 1 values, respectively, as illustrated in figure 1. In this case, M1 and M4 are ON and M2 and M3 are OFF. During the hold time, when WL is 0, M5 and M6 are OFF. In this state, the leakage current through M3 can proportionally lead to failure, since in the idle mode the leakage current through M2 and M5 causes a small increment in the voltage of node X, which is not acceptable due to small SNM in sub-threshold region.

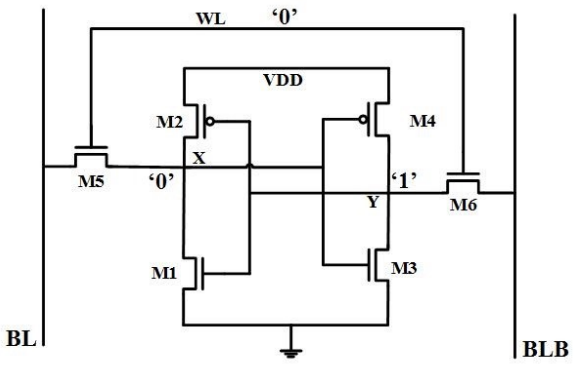


Figure 1. 6T SRAM cell

During the read cycle, when WL=1 and BL=BLB=V_{DD}, M5 and M6 are ON and consequently, BL will be discharged through M1 and M5, and read operation is accomplished. In this situation, due to existence of some leakage through M3 there is a drop in Y, which results in reading speed degradation and possible data flips on storage nodes. In addition, transistor sizing is not adequate to prevent failures, especially in near- and sub-threshold regions [13].

The 11T SRAM cell [14], illustrated in figure 2, improves the whole energy consumption, the ability of working in sub threshold supply voltages the SNM of the 6T SRAM cell but with the penalty of higher number of transistors and larger area. However, the power consumption specially static power, is the critical challenge in designing digital systems especially in SRAMs.

As the 11T and 13T SRAM cells [14] focus on reducing the static power consumption and improving the performance at sub-threshold region, we discuss these cells in more detail. In the 11T cell, M2, M4, M5 and M6 transistors keep the aforementioned characteristics of the 6T cell. However, the size of the M1 and M3 transistors are scaled down equal to the size of the p MOS transistors. In addition, separate BL, WL and RDWL (read word line) lines are considered in this cell, which leads to separated read and write ports.

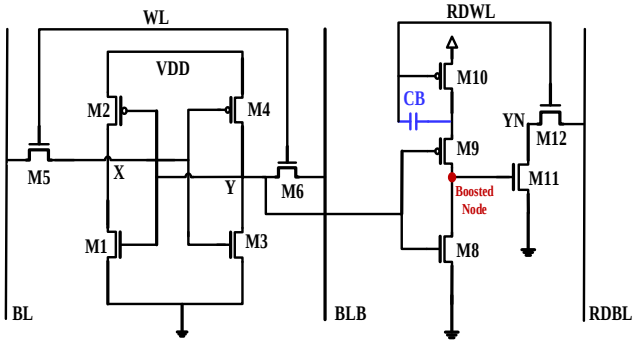


Figure 2. The 11T SRAM cell [12]

During the hold state, the WL and RDWL lines are not activated. Suppose the situation when Y=0 and X=1, as described before for the 6T cell. In the additional 5T circuitry, M12 is OFF and the state of M11 depends on the voltage at node Y. When Y=0, M8 is OFF and M9 is ON, and consequently the gate of M11 is charged. Therefore, a path is created through M11 that connects the node YN to zero. The transistors of the added 5T circuit have minimum size, except the access transistor (M12) that has a larger size.

The boost capacitor (CB) that connects the source of M9 to RDWL is a substantial part in this cell. Given that Y=0 (during the hold and write times) and RDWL is connected to ground, CB starts to charge up to V_{DD}. Though, the amount of charging is limited by M9 and finally the maximum voltage reaches $V_{DD}/2$. Thus, the gate of M11 is connected to a voltage of approximately less than $V_{DD}/2$ and YN discharges to the ground slowly.

When RDWL is selected, the source of M9 rises to 1.5 V_{DD} and the gate of M11 connects to a voltage higher than V_{DD}. This enhances the read current by an order of magnitude as compared to the classical 6T SRAM cell, which leads to faster read operation. In the other case when Y=1, M8 is on and M11 is off, which makes the reading path isolated from the ground. Although the leakage through M11 causes some reduction in the RDBL voltage, this leakage has no effect on YN or RDBL because of connecting M9 to ground via M8.

To suppress the channel leakage path through M8, a modified topology denoted as 13T cell is suggested in [14]. This cell which has 13 transistors is shown in figure 3. When Y is high the source of M8 is connected to ground through the added inverter, but when Y stores “0”, the source of M8 is connected to V_{DD}, which suppresses the leakage path in M8 during the read cycle.

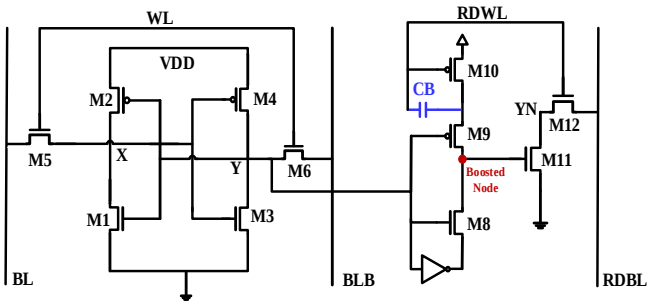


Figure 3. An improved 11T SRAM cell (13T SRAM) [12]

3. Proposed Design

Design of low-voltage digital circuits operating in near- or sub-threshold regions has emerged as a low-power solution for applications with energy constraints. As SRAM memory constitutes a significant percentage of the whole power and area of most digital chips, reducing its power consumption, especially at the stand-by mode, is quite important.

As stated before, the 6T SRAM cell is not suitable for low-voltage applications as it has a small SNM. Accordingly, some effective solutions for improving its SNM in low voltages have been presented in the literature [14]. Despite the improvements in SNM, adding 5 to 7 transistors to the 6T SRAM cell increases the hardware overhead, and consequently the delay and power consumption in the memory system. As a result, for designing an SRAM that maintains the aforementioned SNM improvements, while restricting the hardware redundancy, delay and power, a new hierarchical SRAM (HSRAM) cell is proposed in this paper. The proposed SRAM cell is shown in figure 4. In the proposed design, the hierarchical style also reduces the cell power consumption by use of a multiplexer in the reading path. In this design, due to separating the reading part from the cell, no current is drawn for reading from the cell. Unlike the 6T cell, the read SNM of the proposed cell is not degraded, and is similar to its hold SNM.

As illustrated in figure 4, for reducing the hardware overhead in the 11T SRAM, instead of adding five transistors for each cell, these 5 additional transistors can be shared between each two cells. In this design, the read lines are connected to each other, and the write lines for each cell are separate, as the write ability should be provided for every cell in an SRAM. In order to read from these SRAM cells, a transmission gate-based 2:1 multiplexer is utilized, which connects the SRAM core cells to the read stage. It is worth mentioning that by connecting the read lines, the data stored in each core cell does not become faulty and it is not corrupted during the read procedure.

In the read state, the read line is activated for each of the two cells, and the multiplexer connects the corresponding core cell to the 5-transistor read stage based on the selector signal. If the selector signal becomes '0', the first cell is chosen; otherwise, the second cell is selected. It is noteworthy that the transmission gate structure of the multiplexer provides low-resistive paths and full-swing signals for the read stage.

In addition, the additional inverter existing in the original circuit [14] is omitted in the proposed design as it does not have any considerable effect on the static power, while omitting these two transistors reduces the overall switching power of the SRAM. It is worth pointing out that sharing the read stage also leads to a considerable reduction in the read bit line (RDBL) and read word line (RDWL) capacitances, and consequently results in lower dynamic power consumption and higher speed.

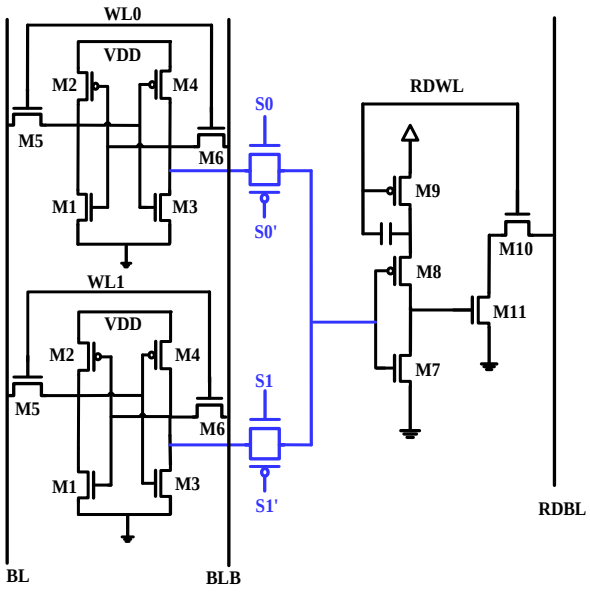


Figure 4. The proposed SRAM (HSRAM)

By categorizing the memory cells and integrating the read line, changing the addressing model of the SRAM cells is necessary. As there is one read line activation for each two cells, according to the conventional models, some clusters of cells may be activated and put on the output simultaneously, which leads to data collision. For solving this problem, the address is divided into two 2-bit parts.

The least significant bit is used as the selectors of the clusters. This bit can be 0 or 1, which will select one of the two cells of each cluster, and the remaining bits will choose the corresponding cluster, and accordingly the corresponding cell is selected to put its data on the output line. These two addressing models are illustrated in figure 5.

4. Simulation Result

The circuits are simulated using the HSPICE simulator tool with 10nm LSTP FinFET technology [15] at 0.45 V supply voltage and at 60°C temperature. Some of the important parameters of the utilized model are given in table 1. In the simulations, all the SRAM's transistors have the minimum size except the ones in the 6T conventional SRAM cell, which have multiple sizes in order to have a good Read SNM. The capacitors of the BL, BLB, RDBL and RDWL lines are assumed as 10fF for a basic design. The power consumption, read and write delays, average case power delay product (PDP), best case PDP, worst case PDP and SNM of the proposed SRAM cell are calculated and compared with those of the other low-power SRAM cells.

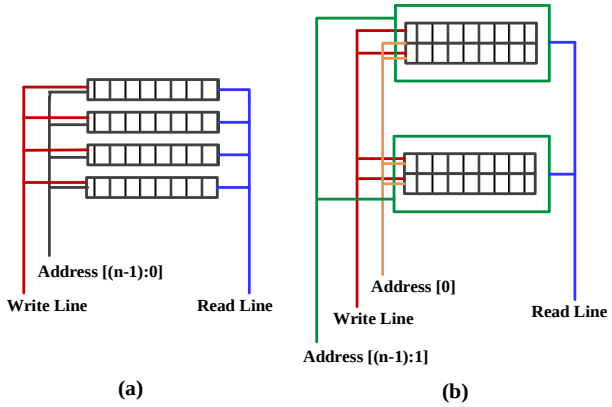


Figure 5. Two addressing models: (a) Conventional model (b) HSRAM Model

Table 1. The FinFET parameters

Parameter	Description	Value
L_g	Physical Gate Length	14 nm
H_{Fin}	Fin Height	21 nm
T_{Fin}	Fin Thickness	8 nm
EOT	Equivalent oxide thickness	0.68 nm
N_{body}	Doping of the body	2.5×10^{16} cm^{-3}
N_{sd}	Doping of the source-drain regions	3×10^{20} cm^{-3}
Φ_{gn}	Work Function of the gate for N-type Transistor	4.42 eV
Φ_{gp}	Work Function of the gate for P-type Transistor	4.75 eV

The simulation results for all SRAM cells are given in table 2 Average PDP is the multiplication of average power and average delay. Best case PDP stands for the product of the average power and best delay, while worst case PDP stands for the product of the worst dynamic power and the worst delay. According to the results, the proposed cell has lower power, write delay and PDP than the other designs. This is because of different structure and operation as compared to 6T, and lower number of transistors and less line capacitance in comparison with 11T and 13T cells.

Table 2. The simulation results at V_{DD}=0.45V

SRAM	Average Power (nW)	Static Power (pW)	Read Delay (ps)	Write Delay (ps)	Average Case PDP (aj)	Best Case PDP (aj)	Worst Case PDP (aJ)
HSRAM	24.81	286.04	311.85	173.11	5.3080	3.8930	19.72
6T	25.60	307.30	319.46	212.64	6.6243	4.7376	20.86
11T	52.91	274.98	244.31	173.86	10.216	8.4497	33.16
13T	36.81	298.11	245.08	177.27	7.1120	5.8346	23.08

Read access delay, which is the time required to discharge RDBL to "0.8×V_{DD}" after RDWL reaches to $V_{DD}/2$, is one of the metrics in SRAM cells. During read operation, RDWL is activated and the access transistor is turned on. If the data which is going to be read is '0', then RDBL will be discharged to ground; and if the data is '1', no change happens in RDBL. According to the results, the read delay access of the proposed HSRAM is 27.24% and 21.65% longer than those of the 13T and 11T SRAM cells, respectively, due to the multiplexer stage, but 2.37% lower than the 6T SRAM since it has a separate read circuitry. However, the proposed method considerably improves the power consumption and PDP metrics as compared to other cells.

Another important metric in evaluation of SRAM cells is the write access delay, which is defined as the time required to charge the node that has stored 0 to $V_{DD}/2$ after WL reaches to $V_{DD}/2$. During write operation, WL is activated and access transistors are turned on. Then, new data is transferred by these transistors to cell. Write delay access of the proposed HSRAM is 2.4%, 0.43% and 22.8% lower than the 13T, 11T and 6T cells, respectively. In the 6T SRAM, in order to have read ability, the size of transistors are different, and therefore, they do not have the same strength. On the other hand, as the pull down transistors have higher strengths than the access transistors, the write delay gets longer.

The delay, power consumption and PDP of the cells versus supply voltage are plotted in figure 7 and figure 8, respectively. According to the results, the proposed cell has lower power consumption and PDP as compared to the other cells in a wide range of supply voltages, especially at lower voltages.

Static noise margin (SNM) is an important metric in evaluating the robustness of an SRAM cell. The SNM parameter is calculated as the diameter of the biggest square found in the butterfly graph of a SRAM cell. For analyzing SNM, Monte Carlo analysis with Gaussian distribution with 10% variation at the 3-sigma is conducted. Process variations are considered in the Fin height, Fin width and channel length as the important FinFET device parameters. Finally, the diameter is measured in the butterfly graph. The butterfly graphs indicating the hold and read SNMs of the propose SRAM cell are illustrated in figure 7.

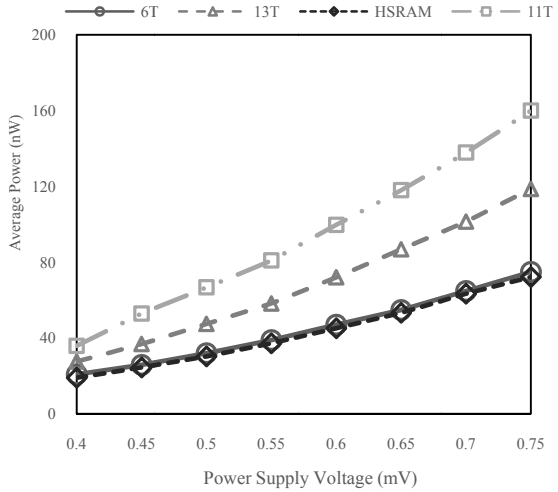


Figure 6. Average Power of the FinFET SRAM cells (T = 60 °C)

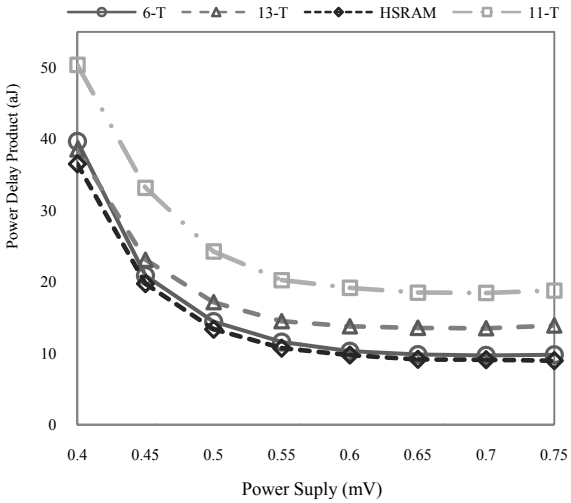
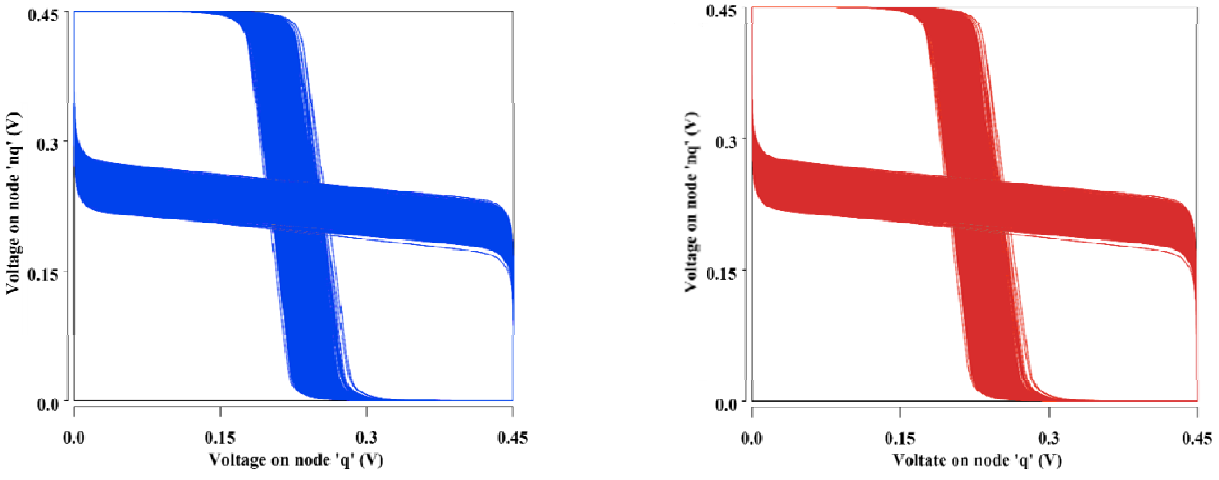


Figure 7. PDP of the FinFET SRAM cells (T = 60 °C)



(a) (b)

Figure 8. The butterfly curves of the proposed cell (a) Hold (b) Read

Table 3 gives the hold and read SNMs, as well as their variations for the SRAM cells. According to table 3, the hold SNMs for all cells are almost comparable. In the read state, the proposed cell as well as the 11T and 13T cells has SNMs equal to their hold state as there is no charge sharing between the separated read bit line and the main cell. However, in the 6T SRAM cell, due to connecting the cell to BL and BLB, the pulling current (charge sharing) from the cell decreases the read SNM.

Table 3. SNM of the SRAM Cells (V_{DD}= 0.45 V)

SRAM Cell	SNM (mV)	Variation (mV)
Hold		
HSRAM	183	34
6T SRAM	182	34
11T SRAM	182	35
13T SRAM	182	35
Read		
HSRAM	183	35
6T SRAM	78	41
11T SRAM	182	35
13T SRAM	182	35

5. Conclusion

In this paper, a hierarchical FinFET SRAM cell (HSRAM) has been proposed. In this design, each two 6T SRAM cells share an additional five-transistor circuitry to improve design complexity and power consumption, and achieve higher SNM and execution speed in sub-threshold region. For reading from these SRAM cells, each two cells are connected to the shared read circuitry through a 2:1 multiplexer and finally to the SRAM output. It is worth mentioning that by connecting the read lines, the data stored in every cell does not become faulty, and is not corrupted during the reading procedure. The SRAM cells have been simulated using 10nm LSTP FinFET HSPICE model. It was shown that the proposed structure reduces the number of transistors, line capacitance, power consumption and PDP as compared to its counterpart cells.

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