

FinFET Based Level Converter for Multi- V_{DD} System Design

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Abstract

Low-power design is the most demanding for nanoscale integrated circuits design. Aggressive low-power design to maximize the battery life is a significant challenge especially in battery-powered digital VLSI systems. Multi- V_{DD} design is an effective approach for low power design. However, in these Multi- V_{DD} systems, the existence of voltage Level Converters (LCs) between these different voltage islands is necessary. Designing low power and low cost LC is a significant challenge to reduce the LCs overhead in multi- V_{DD} systems. In this paper a Single-Supply Level Converter (SSLC) based on independent-gate FinFET is proposed. In the proposed technique, the back gate of FinFETs is biased for providing multi-threshold voltage (V_t) design in order to reduce the number of required transistors in converting low-voltage input signals and decrease static power consumption. Simulation analyses utilizing 22nm technology model demonstrate a qualified performance of the proposed low area and low power design compared to the other previously published most efficient designs.

Keywords: Multi- V_t , Low-Power Design, Single-Supply Level Converter, Independent Gate FinFET, Multi- V_{DD} .

1. Introduction

The nanometer technologies provides the growing integration density of VLSI circuits. However, high power density and higher temperature are produced in the chip. Decreasing supply voltage results in the dynamic power reduction quadratically. In order to decrease the power consumption without degrading the needed performance of an integrated circuit an attractive approach is multiple supply voltages (multi- V_{DD}) design. In these designs, for each different block, based on required performance, a suitable supply voltage is adopted [1, 2].

Ultra-low voltage (ULV) or near the threshold voltage design is more effective for considerably lower power consumption. Nowadays, power minimization is becoming very significant especially in the portable electronic devices (PED). Some specific Portable devices such as personal digital assistants (PDA), laptops, cell phones, digital cameras, micro-sensor nodes, radio frequency identification (RFID) and implantable medical devices demand long battery lifetimes. The limited lifetime of the battery strongly

depends on the average power consumed by the system [3, 4].

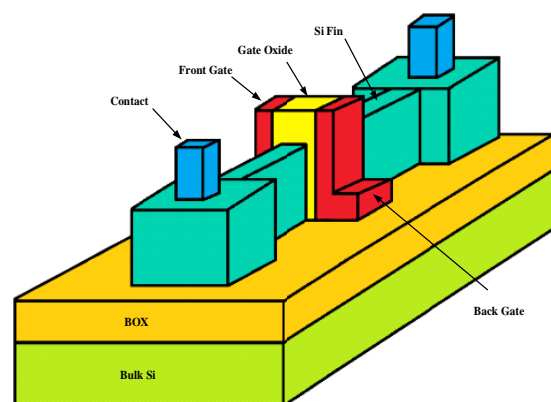


Figure 1. Independent-gate (IG) FinFET structure

When an input signal at logic '1' state is sent from the low voltage (V_{DDL}) circuit to high voltage (V_{DDH}) circuit, the p-type transistors in the pull-up network of the V_{DDH} circuit isn't turned OFF completely and consequently the static

current is increased. However, in multi- V_{DD} circuits, in order to avoid enormous static current, voltage level Converters (LCs) as an interface between these V_{DDL} and V_{DDH} circuits are required. In addition, circuits work at ultra-low supply voltage, for sending signals to I/O circuits require LCs as interconnect. Hereupon, designing most efficient LC with low power, low area and high performance, is an effective challenge in these designs to reduce the LCs overhead [1].

There are two general types of voltage level converters called single supply level converter (SSLC) and dual supply voltage level converter (DSLCL). The advantages of SSLC over DSLCL are less complexity and crowding in supply-voltage routing and lower overall cost of the system [1, 2, 5].

By scaling down the feature size of complementary metal oxide semiconductor (CMOS) technology, due to high lateral electrical field, the short channel effects (SCEs) become more serious, as the supply voltage couldn't be scaled according to the channel length scaling. Significant problems such as high power density, high leakage currents, and enormous parametric variations restrict the scaling down of the CMOS technology for high-density, high-performance and low-power digital VLSI design. In order to alleviate these limitations and challenges, some beyond-CMOS nanodevices such as CNFET (carbon nanotube FET), single electron technology (SET), quantum-dot cellular automata (QCA), and FinFETs (as seen in figure 1) have been introduced as alternatives for conventional bulk-CMOS technology in the near future [6-9].

In the continuous evolution and enhancement of bulk CMOS technology, FinFETs have been proposed as an alternative for alleviating the challenges imposed by continued scaling. The fabrication of FinFETs is compatible with that of conventional CMOS, therefore causing very rapid deployment to manufacturing. FinFET devices have been proposed to overcome the manufacturing limited of planner double-gate devices. In FinFETs, the gate oxide is formed on both sides of the fin simultaneously, which solves alignment problems of source and drain junctions and simplifies the manufacturing process. Additional gate is expected to suppress SCEs and enhance I_{on}/I_{off} ratios by increasing electrostatic stability. Also, utilizing a lightly doped channel in FinFETs causes them resistant to random dopant variations [9].

In this paper, an SSLC based on the independent-gate FinFET is designed for low power applications. The rest of this paper is organized as follows: In section 2 a brief review of IG FinFET is described. Section 3 reviews the previous LCs. Section 4 presents the proposed SSLC design. Section 5 contains the simulation results and comparisons at 22nm technology nodes and finally, section 6 concludes the paper.

2. A Brief Review of Independent-Gate FinFET

Early double-gate devices were manufactured using planar technology suffers from several limits of manufacturing, such as self-alignment of the front-gate and back-gate and the lack of an area efficient contact to the back-gate. FinFET devices have been proposed to overcome the manufacturing problems of the double-gate devices.

Independent-gate (IG) FinFETs can be fabricated along with conventional shorted-gate (SG) devices on the same die

by etching the top part of the FinFET as shown in figure 1. Since the thickness of the silicon fin is small, the electrostatic coupling between the gates is high, and the channel formation in one gate is highly dependent on the state of the other gate. When the back-gate of an IG FinFET is disabled, not only is no channel formed near the disabled gate, but the threshold voltage of the other gate is also increased. Hence, disabling one gate reduces the drive strength of the transistor by more than half. Hereupon, (IG) FinFETs are suitable for dual threshold voltage (V_t) low power design. The back-gate of n-type and p-type devices are disabled by applying zero and VDD, respectively.

The H_{Fin} acts as the Fin height and T_{Fin} is the thickness of Fin. Thus, in the IG FinFET with two gates, the effective gate width is:

$$W_{Effective} = n_{Fin} \times 2 \times H_{Fin} \quad (1)$$

Where n_{fin} is the number of parallel Fins.

The effectiveness of asymmetric independent-gate FinFET depends on how much the front-gate threshold voltage (V_{t-f}) can be changed by modulating the back-gate voltage (V_{bg}). Front-gate threshold voltage can be approximated to have a linear dependence on V_{bg} [10]:

$$V_{t-f} = V_t - rV_{bg} \quad (2)$$

where r is the gate-to-gate coupling factor and is given by:

$$r = \frac{3t_{ox-f}}{3t_{ox-b} + t_{si}} \quad (3)$$

Where t_{ox-f} and t_{ox-b} are the front-gate and back-gate oxide thicknesses, respectively. As the V_{bg} in an IG FinFET can be used to linearly modulate the V_{t-f} , this event can be used to decrease the leakage power of the logic gate. Hence, in this work, IG FinFET is utilized in multi- V_t low power design.

3. Previous Designs

Designing an efficient LC with low-power, high performance and less transistor count has an impressive influence on the overall cost and performance of multi- V_{DD} circuits.

The previously presented LCs require high number of transistors, consume higher power and have lower conversion speed for converting ULV inputs to high voltage outputs. Among the existing digital LCs, most efficient, low-voltage and low-power designs are selected for being reviewed and compared in this work. The DSLC1 of [11] with two main stages is shown in figure 2. The first stage utilizes a cross-coupled differential latch (M_1 , M_2 , M_3 , and M_4) with diode-connected NMOS (M_5). M_5 transistor makes a threshold voltage (V_t) drop for the supply voltage of the cross-coupled latch. So, M_5 has an equivalent to further increasing V_t for PMOS M_3/M_4 transistors. Also, the V_t for M_4 and M_3 are chosen high. These techniques help to weaken the M_3/M_4 compared to M_1/M_2 transistors. Because, for converting ULV inputs, the strength of input transistors M_1/M_2 should overcome the PMOS M_3/M_4 transistors. The second stage is a normal cross-coupled differential latch whose only purpose is converting the output of it from

(0 to $V_{DDH}-V_{t_{M5}}$) range to full-swing output (0 to V_{DD}). Therefore, the majority of up-conversion for low-voltage inputs.

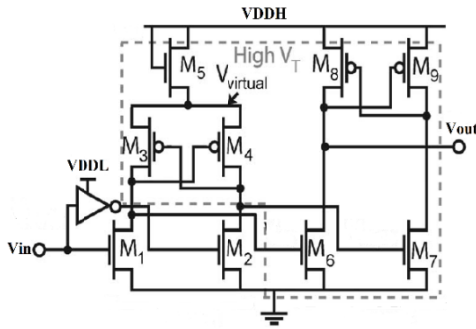


Figure 2. Schematic of the DSLC1 in [11]

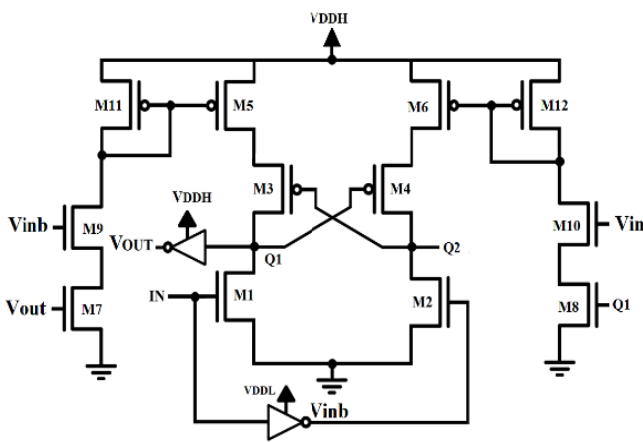


Figure 3. Schematic of the DSLC2 in [12]

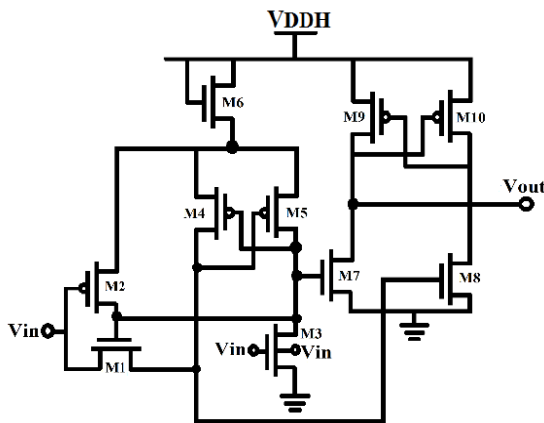


Figure 4. Schematic of the SSLC1 in [13]

Occurs in the first stage. Accordingly, in order to decrease leakage currents, the V_t of first stage transistors are adopted properly.

DSLCC of [12], shown in figure 3, is another cross-coupled level converter which requires dual supply voltages. In DSLCC2 when the input signal is at logic '0', although the M_5 and M_3 transistor are ON and lead to charge of the node Q1, the total charged voltage is lower than V_{DDH} .

This is due to the fact that, when the voltage at node Q1 crosses the switching threshold voltage of the output inverter, the output voltage of inverter (Out) commences to discharge.

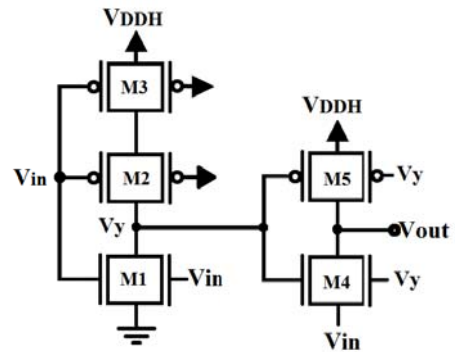


Figure 5. Schematic of the proposed IG FinFET based SSLC

Accordingly, before the voltage of node Q1 reaches V_{DDH} , the output voltage is zero. As a result, the M_7 transistors turns OFF completely that makes M_{11} turned OFF and consequently, M_5 is also turned OFF. Therefore, the node Q1 is not continuously charged to reach V_{DDH} . Nevertheless, this incomplete voltage lower than V_{DDH} of node Q1 is not able to turn OFF the PMOS transistor of this inverter. As a result, static power dissipation is increased specially at small technology node.

In the SSLC1 design of [13] shown in figure 4, in order to up-convert ULV signals, the V_t for M_4 and M_5 is increased by the diode-connected NMOS (M_6) and connected body node of M_3 transistor to V_{in} . So, the cross-couple latch consist of M_7 , M_8 , M_9 and M_{10} transistors is required for full-swing output.

DSLCC1 and SSLCC1 utilize diode-connected NMOS transistors in order to be able to create high V_t pull-up PMOS transistor to increase the strength of input NMOS transistors for up-converting ULV input signals. Then, the second-stage circuit is added to provide full-swing output. So, the number of required transistors is increased and the speed of circuits is decreased.

DSLCC1 and DSLCC2 utilize two supply voltages that increase the overall cost of system and congestion in supply voltage routing. Also, in these DCLCs, the low-supply voltage (V_{DDL}) must track the voltage level of input signal for correct level converting, which increases the sensitivity of these multi- V_{DD} systems.

The SSLC design in [14] with double-gate MOSFET, decrease the utilized transistor by biasing back gate. But, double gate designs, suffer from several limits of manufacturing, such as self-alignment of the front-gate and back-gate and the lack of an area efficient contact to the back-gate. Also, another level converter of [15] utilizes additional logic and supply voltage and extra transistor count to convert low voltage signals that increase the power consumption, delay, supply voltage routing, cost and area of the design.

4. The Proposed Design

LCs occupy redundant area on integrated circuits and also affect the total performance and power consumption of the circuits. However, while reducing the power consumption, LCs should not degrade the minimum required performance of the system. Hereupon, designing a ULV LC with lower static power consumption, high performance, lower transistor count and robustness is a significant challenge.

The proposed design utilizes IG FinFET to decrease the number of transistors and convert low voltage input signals with lower power dissipation. The back gate of an IG FinFET is often used for tuning device threshold voltage (V_t). By utilizing this feature, suitable low power SSLC with lower transistor count is designed. In the proposed SSLC shown in figure 5, in order to convert ULV input signals, the V_t of the FinFETs are adopted by the back gate bias. However, in the proposed SSLC, for M_4 transistor connecting the input signal to the source node provides lower V_{DS} ($V_{DDH}-V_{in}$ instead of V_{DDH}). Thus, when the inputs signal is '1', V_t of M_4 is increased and consequently the leakage current is decreased. Also, in the proposed design, by stacking the M_2 and M_3 transistors, the leakage current through V_{DDH} to GND is decreased considerably.

5. Simulation Results and Comparisons

In this section, the proposed design (Figure 5) and the previous cells (Figures 2, 3, and 4) are verified extensively. Simulations are conducted based on the IG FinFET model of [16] at 22nm technology for proposed design and 22nm metal gate/high-k bulk CMOS based PTM model of [17] at 22nm for other previous designs using HSPICE. Between other 22nm technologies, this transistor characteristic of model of [17] such as V_t and $I_{DS}-V_{GS}$ curve is near to IG FinFET model of [16]. Hereupon, this model is considered for simulations. In order to have fair comparisons, all cells are optimized in terms of energy efficiency and leakage currents.

In the SSLC1 and DSLC2, the gate length (L) and gate width (W) of all transistors are adopted as $L=22\text{nm}$ and $W=44\text{nm}$. In the DSLC1 with the $L=22\text{nm}$ for all transistors, in order to up convert low voltage input signal, the W of input transistors (M_1 and M_2) are adopted to be 88nm and other transistors have W equal to 44nm. In the proposed design with IG FinFET, the L, H_{Fin} and T_{Fin} of all transistors are 22nm, 36nm and 15nm respectively. Just the input transistor (M_1) has two n_{Fins} and other transistors have one n_{Fin} .

The simulation results, listed in table 1, demonstrate the superiority of the proposed designs especially in terms of static and average power consumptions, conversion speed and power-delay product (PDP). The simulations are conducted at 0.9V supply voltage and at room temperature. As LC circuits are used as interfaces between different voltage islands and at the final stage of low-voltage cores, driving capability is a very significant factor in these circuits. Therefore, a 0.8fF output load (C_{load}) capacitor, equivalent to the input capacitance of a fan out-of-4 (FO4) is considered at the output of each cell. According to table 1 the proposed designs outperform the other cells in terms of power consumption, level conversion delay and power-delay product (PDP).

In the proposed SSLC design, by increasing the input voltage, PMOS transistor (M_2) is weakened. As a result, static power consumption is decreased. In the DSLC1, the V_{DDL} voltage should follow the input voltage state. So, by increasing the input voltage and V_{DDL} , static power consumption is increased. In the DSLC2, non-full voltage swing in the input node (Q_1) of the output inverter, produces higher static power. In the SSLC1, assume input signal (V_{in})

is at logic '1'. At the low input voltage due to M_2 and M_1 transistors, and at the high input voltage due to body biasing of M_3 transistor, leakage current through V_{in} is increased.

Systematic and random process variations are among the most significant challenges ahead of designing nanoscale circuits. In order to investigate the effect of the major process variations on the LC circuits, the Monte Carlo simulation has been conducted. Hereupon, for simulation, in the proposed design, the H_{Fin} , T_{Fin} , L and body doping (N) are modeled together as $\pm 5\%$ to $\pm 15\%$ Gaussian distribution with variation at the $\pm 6\sigma$ level [18]. For the other previous designs at 22nm technology with MOSFET, L, W, t_{ox} and N_{Sub} are modeled as variation parameters According to the results at 0.4V of V_{in} and V_{DDL} , and 0.9V of V_{DDH} , demonstrated in figure 6, the proposed design is robust. Due to lower power and delay, and fewer transistors based on IG FinFET, the proposed design has less sensitivity to process variations.

Table 1. Simulation results for designs at $V_{DDH}=0.9\text{V}$

| LCs | $V_{in}(\text{V})$ | Delay (s) | Static Power (w) | Total Power (w) | PDP(j) |
|----------|--------------------|-----------|------------------|-----------------|--------|
| DSLCL1 | 0.4 | 46.75p | 101n | 1u | 46.95a |
| | 0.5 | 35.91p | 105n | 986n | 35.4a |
| DSLCL2 | 0.4 | 31.86p | 3.2u | 1.26u | 40.31a |
| | 0.5 | 23.6p | 3.1u | 1.14u | 26.9a |
| SSLCL1 | 0.4 | 37.2p | 301.3n | 1.11u | 41.3a |
| | 0.5 | 32.86p | 601.5n | 1.41u | 46.33a |
| Proposed | 0.4 | 52.37p | 78.9n | 624.46n | 32.7a |
| | 0.5 | 37p | 6.5n | 717.1n | 26.5a |

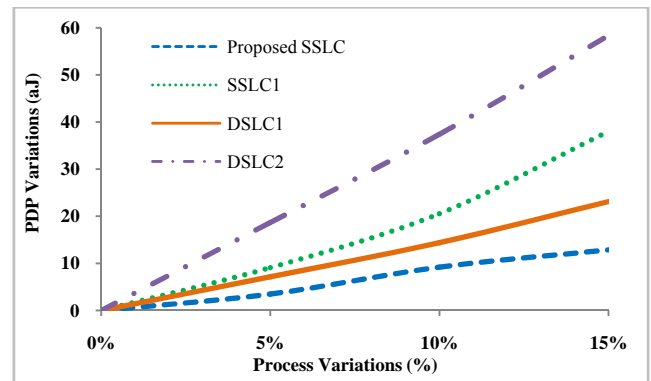


Figure 6. PDP variation of each design in the presence of process variations

In addition to the process variations, supply voltage and temperature variations are presenting a major challenges to the nanoscale integrated circuit design. Requiring low power consumption leads to supply voltage scaling, thus making voltage variations a significant design challenge. Figure 7 demonstrate the PDP of all designs for converting 0.4V input signal in the presence of V_{DDH} variations. The proposed technique for converting the low voltage signal to 0.8v and 0.9V has less sensitivity to supply voltage variations. Whereas, the proposed circuit is designed to convert the input signals to the output voltage of 0.9V as a nominal

supply voltage of 22nm technology, therefore, at 1V supply voltage, the PDP is increased.

The proposed circuit is designed to convert the input signals to the output voltage of 0.9V as a nominal supply voltage of 22nm technology, therefore, at 1V supply voltage, the PDP is increased.

On the other hands, circuit robustness against supply noise is an important metric to take into account when designing a dual- supply system. The gate delay is related to the supply voltage and its sensitivity to supply bounce is increased as the supply is lowered from V_{DDH} to V_{DDL} . Figure 8 demonstrates this sensitivity by comparing the delay variation of the all designs for $\pm 10\%$ supply (V_{DDH} and V_{DDL}) bounce. DSLC2 because of two supplies (V_{DDH} and V_{DDL}), two stages and diode-connected M_3 transistor, has higher delay variation at the presence of supply bounce.

Increasing the power density and higher junction temperature make the temperature variations more critical. Figure 9 demonstrates the PDP of all designs for converting 0.4V input signal at different temperatures. Due to lower power and delay, and fewer transistors, the proposed design has a lower PDP as well as less sensitivity to voltage and temperature variations. In all designs, with temperature increasing, the power consumption is increased and the delay is decreased. However, in the DSLC2 and SSLC1, the power consumption is very sensitive to temperature and increased more. So, PDP in the DSLC2 and SSLC1 is increased with temperature increasing.

6. Conclusion

In this paper, IG FinFET based SSLC had been proposed for being used in the low power digital VLSI systems. The previous LCs, required extra transistors for converting the low voltage input signals. However, in the proposed SSLC, the multi- V_t was provided by properly adopting back gate voltages. Hereupon, the proposed design converted low voltage input signals with lower power consumption.

The proposed design by this technique, utilized only one supply voltage and minimum sized transistors, which improve the manufacturability and robustness of the design. Simulation results demonstrated the robustness and reliability of the proposed IG FinFET based design as well as the superiority of the proposed designs in terms of, power dissipation, speed of level conversion and PDP compared to the other most efficient designs.

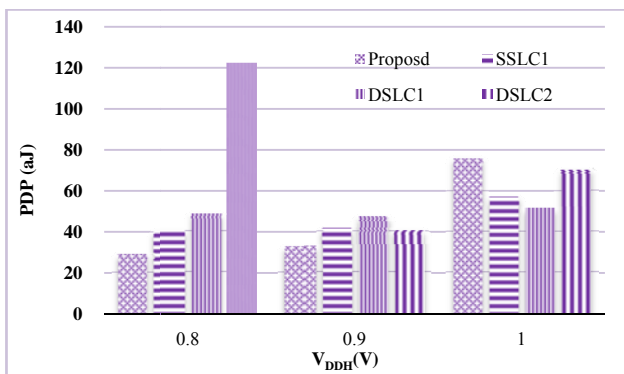


Figure 7. Power-delay product of the all designs at different power supplies

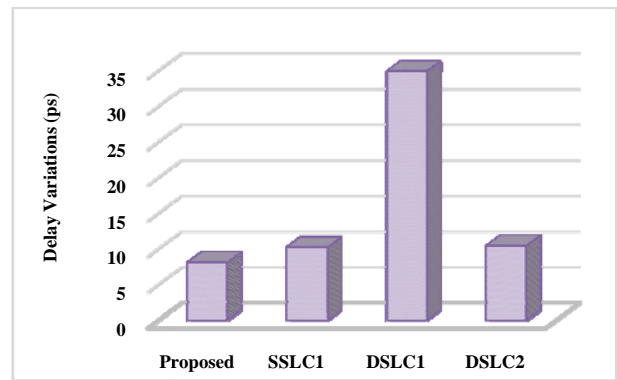


Figure 8. Delay variations of each designs for $\pm 10\%$ V_{DDH} and V_{DDL} bounce

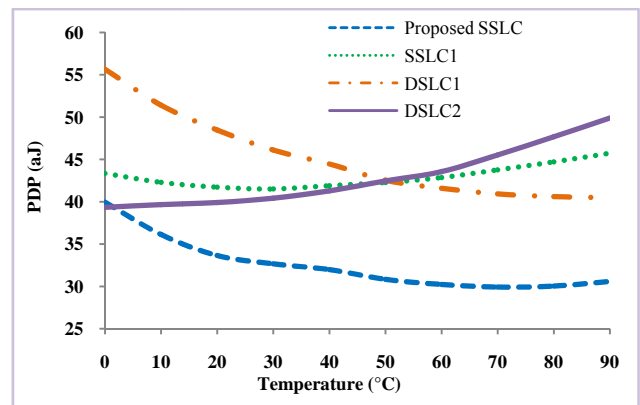


Figure 9. Power-delay product of the all designs at different temperatures

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