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A Two-Stage Method for Optimizing the Parameters of CMOS Operational Amplifiers Based on Evolutionary Algorithm

Seyed Mahmoud Anisheh[1] Chitra Dadkhah[2]

[1]Faculty of Electrical Engineering, K. N. Toosi University of Technology, Tehran, Iran
[2]Faculty of Computer Engineering, K. N. Toosi University of Technology, Tehran, Iran

Abstract

This paper presents a two-stage method for optimization of CMOS operational amplifiers (op-amps) parameters. Modified cuckoo optimization algorithm (MCOA) is employed to evaluate the fitness of every circuit in a generation. Process, voltage and temperature (PVT) variations are considered during optimization. To evaluate the efficiency of the proposed approach, the design of folded-cascode and two-stage op-amps in a $0.18\mu m$ process CMOS technology with 1.8 V supply voltage are presented. The simulation results show the efficiency of the proposed method in determining the parameters of analog circuits.

Keywords: CMOS Analog Circuits, Two-Stage Method, Modified Cuckoo Optimization Algorithm, Folded-Cascode Operational Amplifier, Two-Stage Operational Amplifier.

1. Introduction

Current advances in the VLSI technology have made it possible to integrate analog and digital circuits. The analog portion of a complex mixed-signal system is often smaller than the digital one but it usually demands a considerable portion of the overall design time. This is because there are many parameters, constraints and performances that a designer has to take into account. Therefore, the demand to develop a reliable automatic tool in the design of analog circuits is increasing [1-3].

Analog circuit design consists of three steps: topology selection, parameters optimization and layout generation. First, a designer selects an appropriate circuit topology for a specific application. The second step is sizing devices, in which proper width and length of the MOS transistor, resistor, capacitor values, bias voltages and currents are found. Finally, the layout is obtained from the optimized circuit [4].

A number of optimization computer aided design (CAD) tools in the literature have been introduced in order to determine the sizes of devices. The Steepest Descent method and the Gauss-Newton methods are employed to optimize the parameters of CMOS analog circuits [5]. However, this method suffers from providing local best solutions which do not converge to the global optimum solution. In the knowledge-based approach where a predefined design plan is used, sizes of circuit devices are found in order to satisfy the desired performance specifications [6]. However, this method is time consuming and it cannot ensure the convergence to the global optimum solution. Optimization-based approach can be divided into three categories that are: ‘‘equation-based’’ [7-11], ‘‘simulation-based’’ [12-14] and ‘‘equation and simulation-based’’ [15-17] methods. In the equation-based method, equations are derived by symbolic analyzers to evaluate the circuit performance(s) [7-11]. In the simulation-based method, a circuit simulator is employed to evaluate the circuit performance(s) for a set of design variables [12-14]. Finally, equation and simulation-based method has more accuracy than the equation-based method and it has less computational time than the simulation-based method [15-17]. Method based on gm/I_D which is in the equation and simulation-based category is employed in order to estimate possible solutions and also reduce the search space.

This paper proposes a two-stage method for optimization of CMOS operational amplifiers (op-amps) parameters. Initial solutions are found using analytical equations in order to reduce search space for parameters. Then, the solutions are given to the simulation stage to ensure that the process, voltage and temperature (PVT) variations are within the allocated range. Modified cuckoo optimization algorithm (MCOA) is used for analog circuit design. In this algorithm, transistor sizes, the value of passive components, and the value of bias voltages and currents of the folded-cascode and two-stage op-amps are chosen automatically so that the desired specifications are obtained. This method can also be employed for optimization of the other structures of the amplifiers.

This paper is organized as follows: Section 2 presents the structure of the folded-cascode and two-stage op-amps. The MCOA is explained in Section 3. The design of the folded-cascode and two-stage op-amps using the proposed algorithm is provided in Section 4. Simulation results are given in Section 5. Finally, Section 6 summarizes the results of the proposed method.

2. Op-Amps

Op-amps are essential building blocks of many mixed-mode systems. Since in this research the folded cascade and two-stage op-amps are employed to assess the performance of the proposed method, they are briefly reviewed here.

2.1. Folded Cascode Op-Amp

The folded-cascode op-amp with a p-channel input pair is illustrated in figure 1 [18-19]. It is widely used in high-frequency switched capacitor filters since it has many advantages. In this op-amp, the load capacitor works as a compensation capacitor in order to achieve simple frequency response compensation. Common-mode feedback circuits (CMFB) adjust the common mode output voltage of the op-amp to a desirable fixed reference voltage, typically half of the supply voltage.

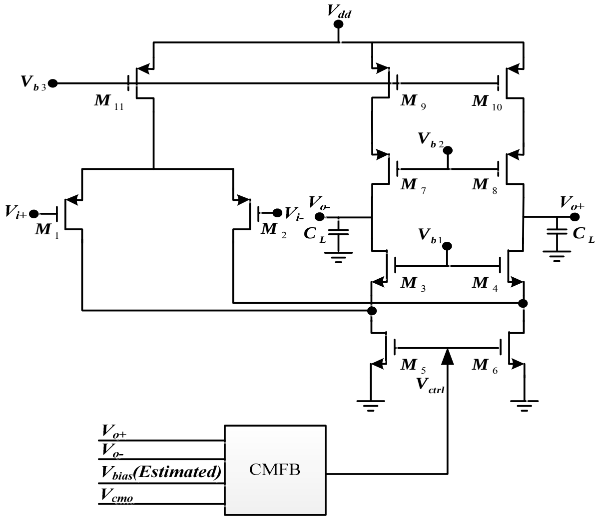


Figure 1. Folded-Cascode Op-amp

The design specifications of the circuit are low-frequency voltage gain (Av), unity-gain-bandwidth (UGBW), slew-rate (SR), power dissipated (P_{diss}), phase margin (PM) and area. The design variables are the transistor sizes (width and length), the value of the passive components such as capacitors and the value of bias voltages. There are several objective functions in designing op-amps that are required to be optimized. These are known as objective or fitness function in optimization literature. Objective functions of folded-cascode op-amp are briefly explained here [18-19].

1) Low-frequency voltage gain

This gain is given by equation (1):

$$A_V = g_{m1}\left\{g_{m8}r_{ds8}r_{ds10} \parallel g_{m4}r_{ds4}\left(r_{ds2} \parallel r_{ds6}\right)\right\} \tag{1}$$

where, g_m denotes the trans-conductance of transistors, Moreover, r_{ds} represents the drain-source resistor of the related transistor.

2) Unity-gain bandwidth

It represents the bandwidth of the circuit and is the frequency in which the gain of the op-amp is equal to 0 dB. This objective has to be maximized based on equation (2).

$$UGBW \cong \frac{g_{m1}}{C_L} \tag{2}$$

3) Slew Rate

This parameter is the evaluation of the circuit capability to respond to any sudden changes. It is desired to maximize SR according to the following equation.

$$SR = \max\left\{\frac{dV_{out}(t)}{dt}\right\} = \frac{I_{D11}}{C_L} \tag{3}$$

4) Power Dissipation

Power dissipation of the folded-cascode op-amp is obtained as below:

$$P_{diss} = V_{dd} \times \left(I_{D9} + I_{D10} + I_{D11}\right) \tag{4}$$

where V_{dd} is the value of the voltage source and I_{D9}, I_{D10} and I_{D11} is the drain current of the transistors M_9, M_{10} and M_{11}.

5) Phase margin

The PM is a measure of relative stability. It is computed by adding the phase value at the unity gain frequency by 180^o. This parameter is calculated as follows (equation (5)):

$$PM = \tan^{-1}\left(\frac{g_{m3}}{UGBW \times C_{gs3}}\right) \tag{5}$$

where C_{gs3} is the gate–source capacitance of transistor M_3.

6) Area

Area is estimated by equation (6):

$$Area = \sum_{i=1}^{k} W_i L_i \tag{6}$$

where W_i and L_i are the width and length of the transistors M_i, respectively.

2.2. Two-Stage Op-Amp

The two-stage op-amp with an n-channel input pair is shown in figure 2 [18-19]. Design specifications are similar to the folded cascade op-amp and are calculated as follows:

1) Low-frequency voltage gain(equation (7))

$$A_V = g_{m1}(r_{ds2} \parallel r_{ds4}).g_{m6}(r_{ds6} \parallel r_{ds7}) \tag{7}$$

2) Unity-gain bandwidth(equation (8))

$$UGBW \cong \frac{g_{m1}}{C_C} \tag{8}$$

3) Slew Rate(equation (9))

$$SR = \frac{I_{D5}}{C_C} \tag{9}$$

4) Power Dissipation(equation (10))

$$P_{diss} = V_{dd} \times \left(I_{D5} + I_{D6}\right) \tag{10}$$

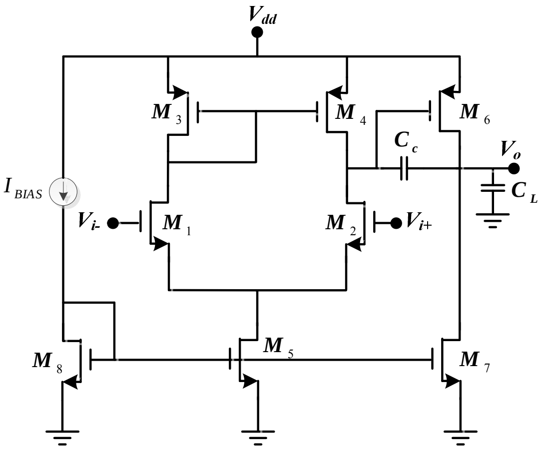


Figure 2. CMOS Two-Stage Op-amp

5) Phase margin (equation (11))

$$PM = 180 - \tan^{-1}\left(\frac{UGBW}{\omega_{P_1}}\right) - \tan^{-1}\left(\frac{UGBW}{\omega_{P_2}}\right) + \tan^{-1}\left(\frac{UGBW}{\omega_{Z_1}}\right) \tag{11}$$

where $\omega_{Z_1} = -\frac{g_{m6}}{C_C}$,

$$\omega_{P_1} = \frac{1}{g_{m6}.C_C\,(r_{ds2} \parallel r_{ds4})(r_{ds6} \parallel r_{ds7})},\ \omega_{P_2} = \frac{g_{m6}}{C_L}.$$

3. Modified Cuckoo Optimization Algorithm (MCOA)

Optimization is the process of searching for the inputs, device characteristics, technical analysis, or experiment to find the best desirable and functional output value. The inputs are variables: cost function, objective function or fitness function. The fitness or cost is the output [20]. The optimization can be implemented by an evolutionary technique that is inspired by the evolution concept in nature to find the best solution of a problem. Various evolutionary algorithms have been proposed in the literatures. One of them is the genetic algorithm (GA) [20] where a number of solutions are considered as candidates. These are called individuals, creatures, or phenotypes which are used to evolve optimization process toward better solutions. Each candidate solution has a set of properties (its chromosomes or genotype), which can be mutated and changed. Usually, solutions are shown in binary as strings of 0s and 1s, but other types of encodings are also possible. The evolution of ten begins from a population of randomly generated individuals. Then, the process is repeated with the population in each iteration which is called a generation. The fitness of every individual in the population is evaluated in each generation. The fittest individuals are randomly selected from the current population and then each individual's genome is modified (recombined and possibly randomly mutated) to form a new generation. These are used in the next iteration of the algorithm. Commonly, the algorithm ends when either maximum number of generations is produced or a desired population fitness level is reached. Another evolutionary algorithm is particle swarm optimization (PSO) which is stemmed from the behavior of a flock of birds or school of fishes or the social behavior of a group of people [21]. Each individual flies in search space with a velocity which is dynamically adjusted by its own and companions' fly experiences. This is different from other evolutionary operators that employ manipulation of individuals.

Cuckoo optimization algorithm (COA) is a new evolutionary method, which comes from lifestyle of cuckoo birds [22]. It is started by an initial population of cuckoos that lay some eggs in host birds' nests. Those are similar to the host bird's eggs have the chance to grow up and become adult cuckoos. Other eggs are detected by the host birds and are assassinated. The grown chicks show the suitability of the nests in that area. Surviving more chicks in an area, the more profit is assigned to the area. So the position in which more eggs survive will be the goal that COA will target to optimize.

The values of problem variables in COA is called "habitat". For example, the ith habitat is represented as $x_i = (x_{i1}, x_{i2}, \ldots, x_{id})$ in the d-dimensional space. Then, some randomly produced number of eggs is assumed for each of these initial cuckoo populations. Real cuckoos lay eggs at a maximum distance from their habitat, which is called "Egg Laying Radius (ELR)". The ELR is defined as equation (12):

$$\mathrm{ELR} = \alpha \times \frac{\text{Number of current cuckoo's eggs}}{\text{Total number of eggs}} \times (\mathrm{var_h} - \mathrm{var_l}) \tag{12}$$

where α is an integer, assume to handle the maximum value of ELR, var_h is the upper limit and var_l is the lower limit of the problem interval. Upper and lower limits depend on the variable limits of the problem and can be defined by the knowledge of a designer. For example, for a gate-source voltage between 0.5 to 0.7 volts, the lower limit is 0.5 V and upper limit is 0.7 V. Large values of $|var_h - var_l|$ increase the computational time of the algorithm.

When a maximum number of iterations is reached, all populations move to one of the best habitat with maximum similarity of eggs to the host birds and also with the maximum food resources. This habitat will produce the maximum profit ever.

This algorithm is summarized as follows:

1. Initialize cuckoo habitats with random points on the profit function
2. Assign some eggs to each cuckoo
3. Define Egg Laying Radius (ELR) for each cuckoo
4. Laying some eggs by cuckoos in their ELR
5. Host bird kill some detected eggs
6. Let eggs hatch and chicks grow
7. Evaluate the habitat of each newly grown cuckoo
8. Limit the maximum number of cuckoos
9. Cluster cuckoos and find best group
10. Migration of the cuckoos toward best group of distance lambda where the lambda shows the percentage of the overall distance
11. Stop when stop condition is satisfied, unless go to step 2

The comparison of COA with standard versions of PSO and GA showed the superiority of COA in fast convergence and global optima achievement [22]. In another research [23], MCOA has been introduced. The main aim of MCOA technique is to gradually reduce the ELR parameter defined in equation (12). This method has been applied to two engineering optimization problems namely pressure vessel design problem and welded beam design problem. Simulation results indicate the superiority of MCOA method compared to conventional COA method.

4. Proposed Optimization Method

The flowchart of the proposed method is shown in figure 3. Initial solutions are provided using analytical equations in order to reduce search space for parameters. Then, the results are given to the simulation stage to ensure that the PVT variations are in the allocated range. The details are given as follows:

Step 1: In the first step, technology model parameters are chosen from the technology file.

Step 2: In this step, design variables of the circuit are specified. For the folded-cascode op-amp shown in figure 1, the variables are: W_1 and L_1 of $M_{1,2}$, W_2 and L_2 of $M_{5,6}$, W_3 and L_3 of $M_{3,4}$, W_4 and L_4 of $M_{7,8}$, W_5 and L_5 of $M_{9,10}$, W_6 and L_6 of M_{11}, V_{b1}, V_{b2}, V_{b3}, V_{bias}, and C_L. Design variables of the two-stage op-amp, shown in figure 2, are: W_1 and L_1 of $M_{1,2}$, W_2 and L_2 of $M_{3,4}$, W_3 and L_3 of $M_{5,7,8}$, W_4 and L_4 of M_6, C_C and I_{BIAS}.

Step 3: Equations (1)-(6) of the folded-cascode op-amp and equations (7)-(11) of the two-stage op-amp are evaluated using MCOA. Weighted sum method has been widely used for multi-objective optimization. It transforms multiple objectives into an aggregated objective function. All functions are multiplied by weighting factors and the results are summed (13):

$$F = \sum_{i=1}^{n} W_i . f_i \tag{13}$$

In the above equation, W_i is the weighting factor for the i^th objective function, and n is the number of objectives. In this research, objectives are Av, UGBW, SR, P_{diss}, PM and area of the op-amps.

Step 4: If the desired specifications are not achieved according to the cost function evaluation, new solutions are searched by MCOA. Otherwise, the solutions are given to the second stage.

Step 5: The net list of the circuit is extracted which is necessary for HSPICE simulation.

Step 6: HSPICE simulation is run to compute the target specifications in the second stage. For this purpose, a new MATLAB toolbox is written. It has the capability to create a net list for HSPICE and run it automatically. Simulation results are obtained from the list file of HSPICE. Then, it computes the target specifications of the op-amps. In this stage, optimization is also performed by MCOA.

Step 7: If the PVT variations are in the allocated range, the algorithm stops. Otherwise, MCOA is looking for new solutions. The process variations are described by corners as Typical (T), Slow (S) and Fast (F) for both types of NMOS and PMOS. Three process and temperature corners TT(27° C), FF(-40° C) and SS(90° C) are used. The voltage variation is $\pm 10\%$ of the nominal value.

Target specifications are optimized using MCOA algorithm. In the MCOA algorithm the following parameters should be adjusted:

1) Number of initial population
2) Minimum number of eggs for each cuckoo
3) Maximum number of eggs for each cuckoo
4) Maximum iterations of the Cuckoo Algorithm
5) Number of clusters that we want to make
6) Lambda variable in COA
7) Maximum number of cuckoos that can live at the same time
8) Control parameter of egg laying
9) Population variance that cuts the optimization

Methods such as penalty function have been proposed to solve constrained optimization in recent researches. The idea in penalty function is to transform the constrained optimization problem into an unconstraint one. It is performed by adding a certain value corresponding to constraint violations to the objective function [24-26]. This method has been widely used due to its convenience and effectiveness. Hence, the penalty function is adopted in this paper. For this purpose, the following penalty method is used to transform the constrained placement problem into an unconstraint optimization problem.

$$Cost = F + w_1 \times (sum\_viol) + w_2 \times num\_viol \qquad (14)$$

where F is the objective function of the problem, w_1 and w_2 are penalty factors, sum_viol denotes the sum of all the amounts by which the constraints are violated, and num_viol denotes the number of constraints violations.

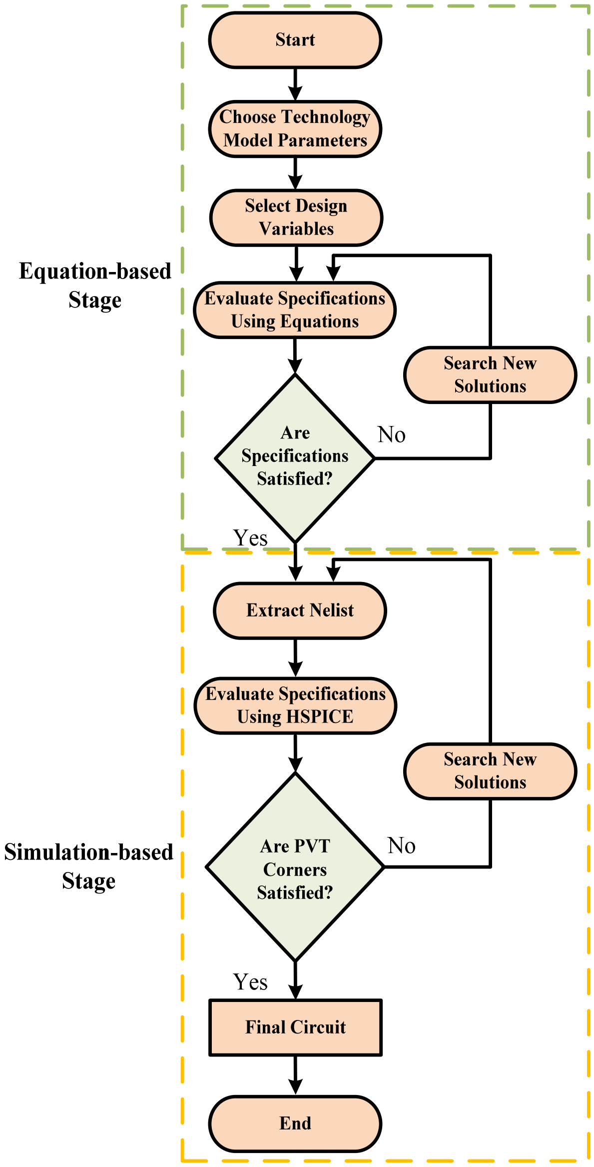


Figure 3. Flowchart of the proposed method

5. Performance Evaluation

The design automation of the op-amps is performed in a $0.18\,\mu$m, 1.8V CMOS technology. For this purpose, a new MATLAB toolbox is written. All optimization programs are run in MATLAB R2013a version and are here tested on Intel(R) core $^{\text{TM}}$ i5-4460 CPU @ 3.2 GHz with 16 GB RAM. In this research, the following MCOA parameters are used:

- Number of initial population = 10,
- Minimum number of eggs for each cuckoo = 5,
- Maximum number of eggs for each cuckoo = 8,
- Maximum iterations of the Cuckoo algorithm = 50,
- Number of clusters that we want to make = 3,
- Lambda variable in COA =2,
- Maximum number of cuckoos that can live at the same time = 60,
- Control parameter of egg laying reduced from 20 to 5,
- Population variance that cuts the optimization =1e-13.

The above parameters are chosen such that there is a compromise between the speed and accuracy of the algorithm.

Desired specifications of the folded-cascode op-amp are shown in table 1. Performance of the proposed two-stage method is compared with the single simulation stage and also the existing method [7]. The design variables which satisfy the specifications of the op-amp are reported in table 2.The obtained design specifications of the folded-cascode op-amp are presented in table 3. As can be seen from the results, the two-stage method can satisfy the specifications. The proposed methods and the existing method are applied to the same circuits with the same technology and the results are compared here. The main advantage of the proposed two-stage method compared with the existing method [7] is that the initial solutions are provided using analytical equations to improve the convergence of the algorithm. The cost functions of the proposed methods after 50 iterations are shown in figure 4 which proves that the two-stage method can converge better than the other. The open loop frequency responses of the op-amp which is designed by the proposed two-stage method, in three process and temperature corners are shown in figure 5 and also are summarized in table 4. A 0.4 V step voltage is applied to the op-amp and the response is demonstrated in figure 6. In addition, $\pm 10\%$ power supply variations effect on frequency responses at TT(27° C) are shown in figure 7. To further evaluate the performance of the proposed optimized op-amp, it has been used in a 80 MS/s flip-around sample-and-hold (SHA) [18-19] with 2 MHz input frequency and an input amplitude of $A_{in,\,diff} = 0.4$V. The schematic of SHA is shown in figure 8.a. The FFT of the SHA output is shown in figure 8.b using 256-points.Accordingly, the calculated total harmonic distortion (THD) is about -80 dB.

Desired specifications of the two-stage op-amp are shown in table 5. The design variables satisfying the specifications and the obtained design specifications of the proposed method with and without first stage are reported in table 6 and table 7, respectively. The results demonstrate the superiority of the proposed two-stage technique compared with the single simulation stage and also the existing method [7]. The cost functions of the proposed methods are demonstrated in figure 9.

Table 1. Desired specifications of the folded-cascode op-amp

No.	Specifications	Desired value
1	DC Gain	>50 dB
2	Unity Gain Bandwidth	>350 MHz
3	Slew Rate	>400 V/µs
4	Phase Margin	$55^o < PM < 65^o$
5	Power Dissipation	Minimized
6	Area	Minimized

The open loop frequency responses of the op-amp which is designed by the proposed two-stage method, in three process and temperature corners are shown in figure 10 and also are reported in table 8. Finally, transient step response of the two-stage op-amp is shown in figure 11.

Table 2. The design variables of the folded-cascode op-amp obtained by the proposed methods and the existing method

Design Variables	**Two-Stage**	**Simulation Stage**	**GA [7]**
W_1 (µm)	46.64×2	50×2	46.23×2
W_2 (µm)	38.87×3	41.67×3	38.53×3
W_3 (µm)	7.78	8.33	7.71
W_4 (µm)	23.32	25	23.12
W_5 (µm)	23.32	25	23.12
W_6 (µm)	93.28×2	100×2	92.46×2
$L_{1\text{-}6}$ (µm) (fixed value is chosen)	0.18	0.18	0.18
V_{b1} (V)	0.91	1.43	0.99
V_{b2} (V)	0.89	0.37	0.81
V_{b3} (V)	1.24	1.27	1.26
V_{bias} (V)	0.62	0.6	0.61
C_L (pF)	1.04	1.14	1.06

Table 3. The obtained design specifications of the folded-cascode op-amp for the proposed methods and the existing method

specifications	**Two-Stage**	**Simulation Stage**	**GA [7]**
DC_Gain (dB)	53.9	46.2	53.4
Phase_Margin (°)	62.9	63.8	64.5
UGBW (MHz)	398	281	285
Power_Dissipation (m W)	1.1	0.74	0.79
Slew_Rate (V/µs)	470	283	320
Area (μm^2)	128	138	127
Total run time (s)	1087	892	1023

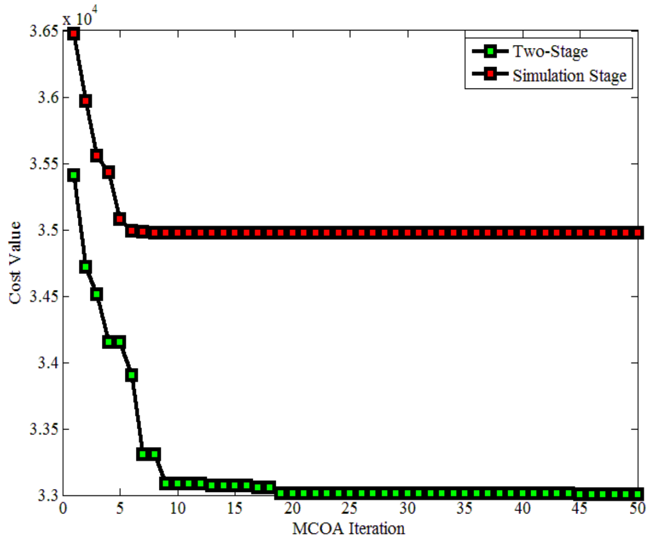
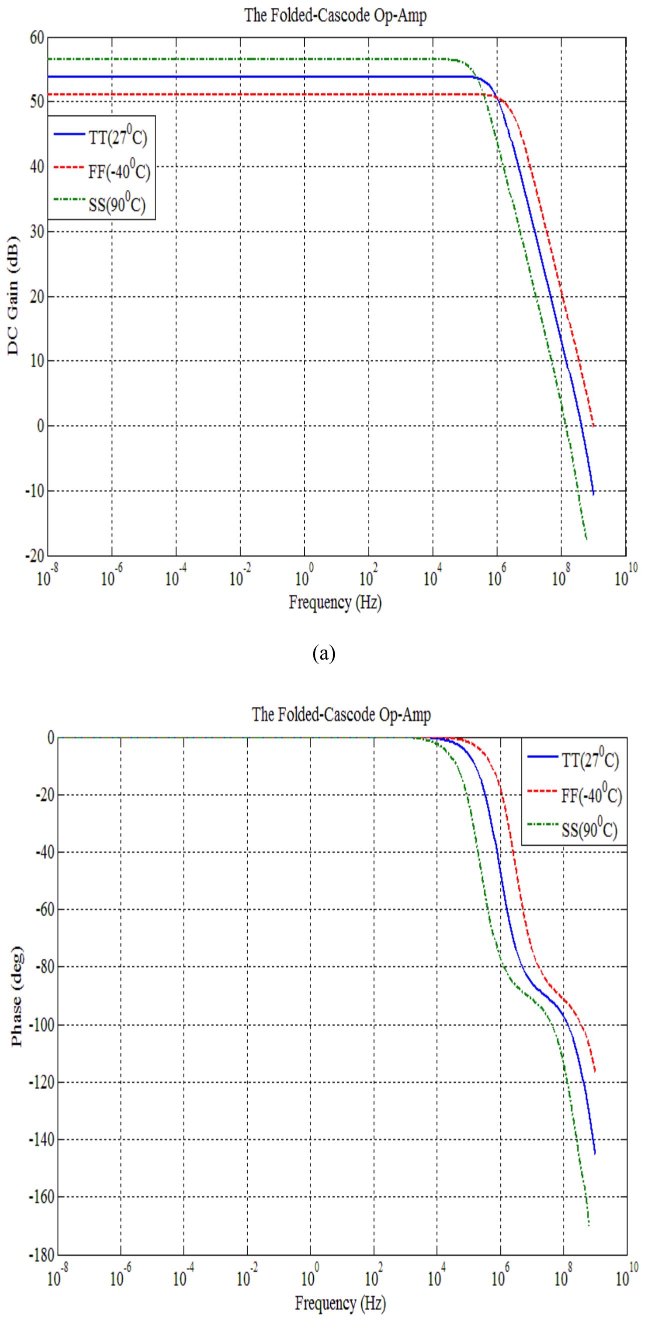


Figure 4. Cost functions of the folded-cascode op-amp after 50 iterations



(a)

(b)

Figure 5. Frequency responses of the folded-cascode op-amp: (a) magnitude and (b) phase

Table 4. Specifications of the folded-cascode op-amp in three process and temperature corners

Specification	Folded-cascode op-amp		
	TT(27° C)	FF(−40° C)	SS(90° C)
Technology	0.18µm	0.18µm	0.18µm
Supply Voltage	1.8 V	1.98 V	1.62V
DC-Gain (dB)	53.9	50.1	56.5
UGBW (MHz)	398	850	157
Slew Rate (V/µs)	470	687	241
Phase Margin (°)	62.9	66	59
Power Dissipation (m W)	1.1	2.3	0.55
Estimated Area (μm^2)	128	128	128
C_L (pF)	1.04	1.04	1.04

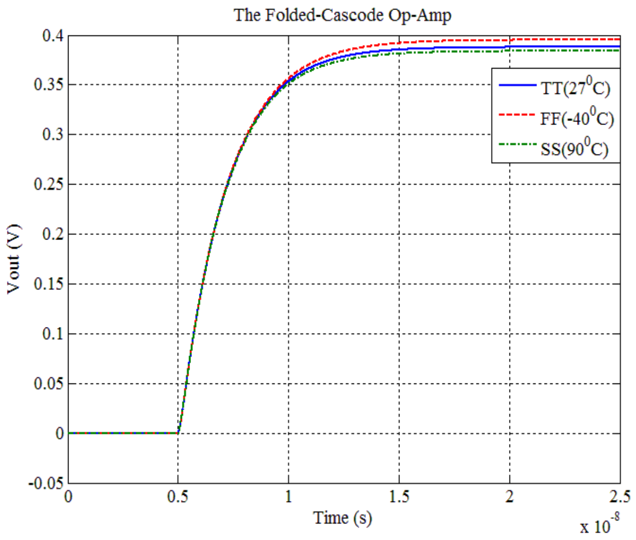
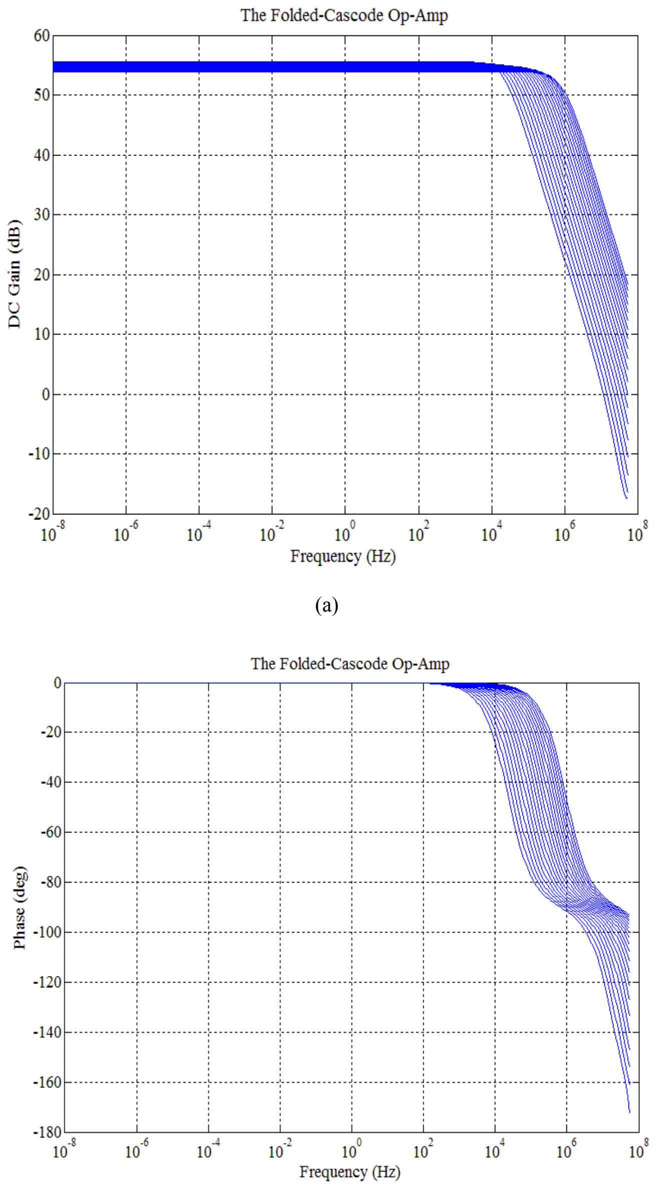


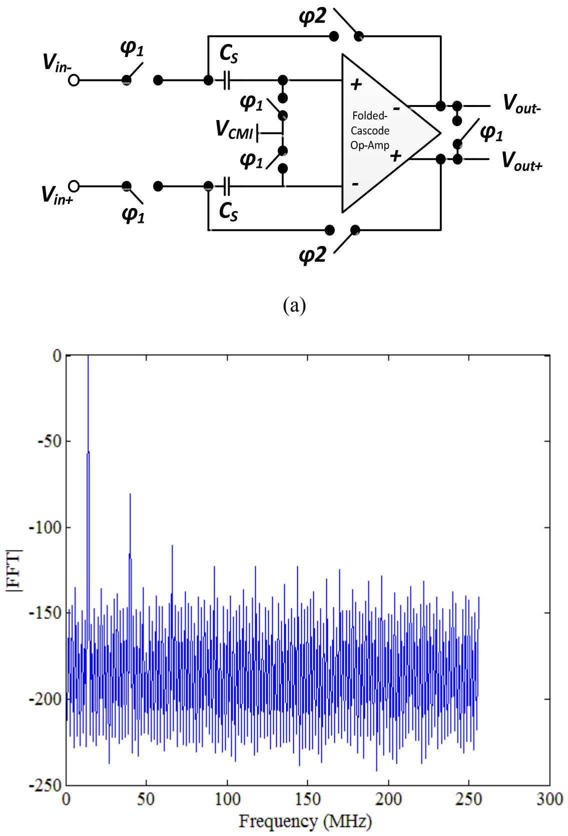
Figure 6. The folded-cascode op-amp step response



(a)

(b)

Figure 7. Power supply variation on frequency response of the folded-cascode op-amp: (a) magnitude and (b) phase



(a)

(b)

Figure 8. a) Flip-around sample-and-hold, b) FFT plot of the output of the sample-and-hold

Table 5. Desired specifications of the two-stage op-amp

No.	Specifications	Desired value
1	DC Gain	>45 dB
2	Unity Gain Bandwidth	>300 MHz
3	Slew Rate	>300 V/µs
4	Phase Margin	$45^o < PM < 55^o$
5	Power Dissipation	Minimized
6	Area	Minimized

Table 6. The design variables of the two-stage op-amp obtained by the proposed methods and the existing method

Design Variables	Two-Stage	Simulation Stage	GA [7]
W_1 (µm)	40.11	31.1	34.76
W_2 (µm)	80.22	62.2	69.52
W_3 (µm)	80.22	62.2	69.52
W_4 (µm)	40.11×6	31.1×6	34.76×6
$L_{1\text{-}4}$ (µm) (fixed value is chosen)	0.18	0.18	0.18
I_{BIAS} (µA)	883	500	717
C_C (pF)	3	2.3	2.7
C_L (pF) (fixed value)	1	1	1

Table 7. The obtained design specifications of the two-stage op-amp for the proposed methods and the existing method

specification	Two-Stage	Simulation Stage	GA [7]
DC_Gain (dB)	48.3	46.9	46.8
Phase_Margin (°)	48.2	48.2	49.4
UGBW (MHz)	316	251	281
Power_Dissipation (m W)	5.4	4.2	4.8
Slew_ Rate (V/μs)	305	232	274
Area (μm^2)	129	100	113
Total run time (s)	810	614	720

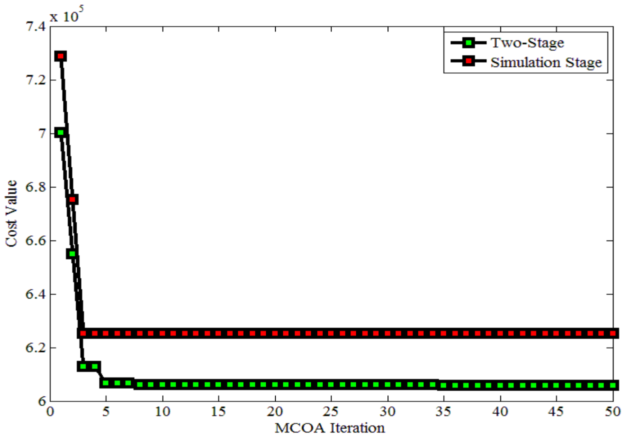
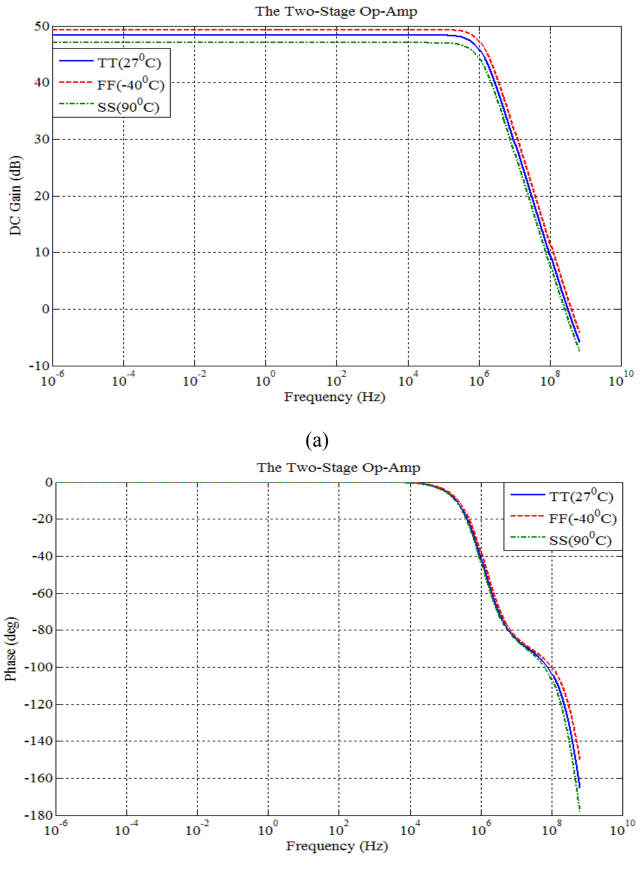


Figure 9. Cost functions of the two-stage op-amp after 50 iterations



(a)

(b)

Figure 10. Frequency responses of the two-stage op-amp: (a) magnitude and (b) phase

Table 8. Specifications of the two-stage op-amp in three process and temperature corners

Specification	Two-stage op-amp		
	TT (27° C)	FF (−40° C)	SS (90° C)
Technology	0.18μm	0.18μm	0.18μm
Supply Voltage	1.8 V	1.98 V	1.62V
DC-Gain (dB)	48.3	49.3	47
UGBW (MHz)	316	423	249
Slew Rate (V/μs)	305	348	277
Phase Margin (°)	48.2	49	48
Power Dissipation (m W)	5.4	5.9	5
Estimated Area (μm^2)	129	129	129
C_L (pF)	1	1	1

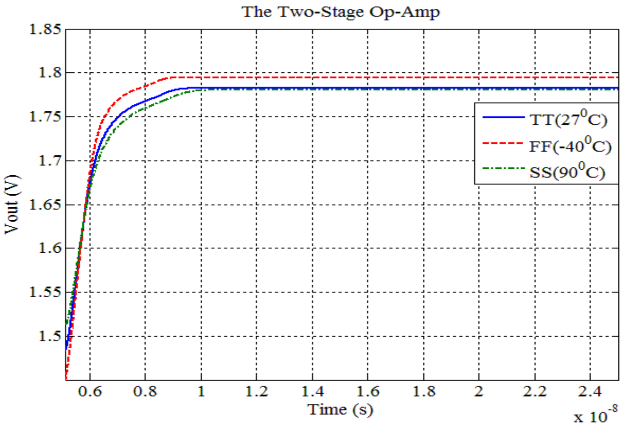


Figure 11. The two-stage op-amp step response.

6. Conclusions

In this paper, a two-stage method for optimizing the parameters of folded-cascode and two-stage op-amps has been proposed. Initial solutions have been found by analytical equations to reduce search space for parameters. Then, the results for PVT variations have been searched by simulation stage to verify whether they were within the allocated range or not. The MCOA was used to assign optimal values for the transistor sizes, the value of capacitors, and the value of bias voltages and currents. In order to evaluate the effectiveness of the system, several simulations have been carried out and the results highlighted the efficiency of the proposed method in CMOS analog circuitdesign.

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Seyed Mahmoud Anisheh graduated from the Amirkabir University of Technology in 2006. He received the M. Eng. degree from the University of Mazandaran, Babol, Iran, in 2009. He is currently working toward the Ph.D. degree in electrical engineering at the Khaje Nasir Toosi University of Technology, Tehran, Iran. His research interests include high performance Op-Amps, automatic analog circuit layout generation, RFIC, and signal processing.

Email: s.m.anisheh@ee.kntu.ac.ir

Chitra Dadkhah received the B.Sc. degree in software engineering from Shahid Beheshti University, Tehran, Iran, in 1990, the M. Sc. degree in computer engineering (artificial intelligence) from the IASI Department, University of Paris 11, Orsay, France, 1993. She also received the Ph.D. degree in computer engineering from the Department of Computer Engineering & IT, Amir Kabir University (Poly technique), Tehran, Iran, 2005. She is Assistant Professor in Computer Engineering Faculty of K. N. Toosi University of Technology, Tehran, Iran. Her research interests include Evolutionary & Swarm Algorithms, Natural language processing, Recommender Systems, Robotic (simulation).

Email: dadkhah@eetd.kntu.ac.ir

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Corresponding author: Dr. Chitra Dadkhah,
Faculty of Computer Engineering, K. N. Toosi University of Technology, Tehran, Iran.