

Integration of CTL, PTL, and DCVSL for Designing a Novel Fast Ternary Half Adder

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Abstract

Differential cascode voltage switch logic (DCVSL) is a well-known and practical logic style, which generates two complementary outputs in parallel. High-speed operation is a great advantage of this logic style. This paper presents a novel ternary half adder by integrating capacitive threshold logic (CTL), pass-transistor logic (PTL), and ternary DCVSL. The new design is tested and evaluated by using the CAD tool HSPICE and 32 nanometer CNFET technology. Simulation results demonstrate rapidness and robustness for the proposed ternary half adder. It operates 6.3% faster, and consumes 0.015 μ W less power than its similar competitor. Moreover, the most beneficial achievement is the elimination of 19 transistors which leads to significant cost and area savings.

Keywords: Half Adder, DCVS, Pass-Transistor Logic, Capacitive Threshold Logic, Ternary Logic, Multiple-Valued Logic, High Speed.

1. Introduction

Binary has been the dominant logic for designing digital circuits over the past decades. However, it cannot correspond to the real-life events whose nature is beyond dualism. Many daily situations such as being warm or cold are relative issues whose definitions require more than two definite states. Furthermore, the congestion of wires inside a digital chip causes some challenges such as complex routing of interconnection [1], coupling effects [2], and high power dissipation [2-3]. A study shows that wires are the source of about 70 percent power consumption inside chips [3]. Multiple-Valued Logic (MVL) can be an appropriate response to the difficulties of binary logic implementation. There are more than two states in MVL, which reduces the amount of wires as well as hardware components. In this way, a wire can carry and a memory cell can store more information [4]. There are several ternary and quaternary circuits in the literature [5-9]. According to [10], the most efficient radix for implementation of a switching system is the natural number e ($e \approx 2.718$). However, it is not in accordance with the intrinsic operation of electronic

elements. Radix-3 has higher performance than radix-2, since it is a closer integer number to e . Nevertheless, ternary logic cannot be successful unless high-performance ternary circuits are presented.

The most well-known logic styles in binary logic are Complementary MOS (CMOS), Pass-Transistor Logic (PTL), Threshold Logic (TL), Dynamic Logic, and Differential Logic. Each one has its own advantages and disadvantages making it suitable for a special application. Differential Cascode Voltage Switch (DCVS) belongs to the differential logic category, where there are always two complementary outputs generated concurrently. Although it usually consumes more power than other competitors, it is fast, robust, and reliable. The inherent redundancy within DCVCL makes it ideal for error detection applications [11]. A ternary DCVSL paradigm has been presented in [12]. Another useful logic style is Capacitive Threshold Logic (CTL), which is based on capacitive summation. It makes the implementation of circuits with fewer transistors possible. For instance, the ternary full adder presented in [6] has only 26 transistors. Another famous logic which reduces transistor count is PTL, where either the pull-up or pull-down network

is eliminated. In addition, it usually forms short paths from the input signals to the output node through and along the critical path of a circuit.

This paper presents a novel ternary half adder by combining the logic styles DCVSL, CTL, and PTL. Carbon Nanotube Field Effect Transistors (CNFETs) are used in this paper to design the new adder cell. It is an emerging technology which is considered as a propitious successor to the current CMOS technology. Previous comparisons show that the CNFET circuits operate faster and consume less power than their CMOS counterparts [13-14]. Furthermore, CNFETs show outstanding characteristics especially for designing MVL circuits. One of the exceptional properties is the ability of individual threshold adjustment of transistors. It provides the necessary flexibility especially for multi-threshold designs. In contrast, MOSFET transistor is inherently a single-threshold device [15].

The rest of the paper is organized as follows: Section 2 provides a brief literature review of ternary DCVSL. Section 3 introduces the only DCVSL ternary half adder cell presented so far. As far as we have searched on the previous studies, there is not any other similar circuit yet, and it is the only available case. The new DCVSL ternary half adder is proposed in Section 4. Section 5 includes simulation results. Finally, Section 6 concludes the paper.

2. Ternary DCVSL

DCVSL is a well-known and practical logic style in binary logic. The structure generates two complementary outputs simultaneously. The overall structure is depicted in Fig. 1. In this model, the main part of the circuit is composed of four transistors: two cross-coupled p-type transistors in the pull-up network (PUN); and two individual n-type transistors in the pull-down network (PDN). The n-type transistors receive dependent X and Y input signals with an exclusive manner (Fig. 1). Please note that there must be one and only one active transistor at the same time. In summary, if $X=V_{DD}$ and $Y=0V$, then $Out_1=1$ and $Out_2=0$ (Fig. 1a). The opposite occurs in the form of Fig. 1b. There are three states '0', '1', and '2' in ternary logic represented by $0V$, $\frac{1}{2}V_{DD}$, and V_{DD} , respectively. The method, which has been presented in [12], transforms binary DCVSL into a ternary model by adding only four resistors (Fig. 2). These resistors are responsible for voltage division between the power supply and ground when the outputs are meant to be '1' ($\frac{1}{2}V_{DD}$). In resemblance to the binary model, the same thing happens if no more than one input signal, X or Y , equals V_{DD} (Figs. 2a and 2b). There is not any determining role for the resistors in these circumstances. However, there is another possibility where both PDNs switch on at the same time ($X=Y=V_{DD}$). This causes simultaneous voltage drop for both outputs, and consequently the

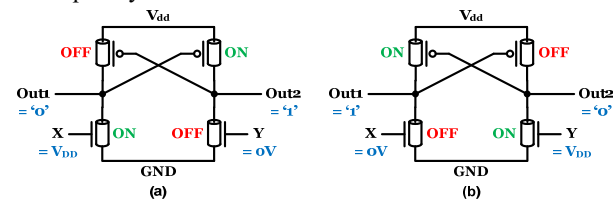


Figure 1: The overall structure of DCVSL in binary logic, (a) $Out_1='0'$ and $Out_2='1'$, (b) $Out_1='1'$ and $Out_2='0'$.

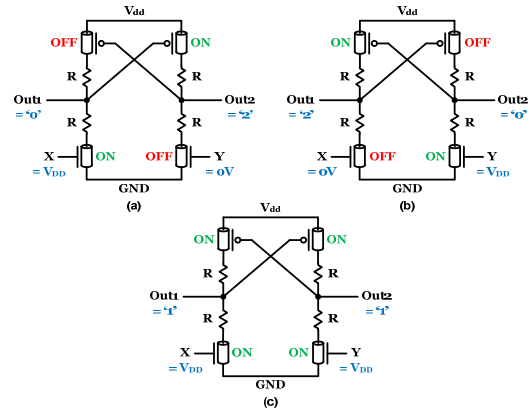


Figure 2: The overall structure of DCVSL in ternary logic, (a) $Out_1='0'$ and $Out_2='2'$, (b) $Out_1='2'$ and $Out_2='0'$, $Out_1=Out_2='1'$.

pull-up transistors turn on as well. Then, the resistors divide voltage and both outputs become '1' (Fig. 2c). The cross-coupled p-type transistors must remain on when receiving logic value '1'.

Fig. 2 illustrates the core architecture of a ternary DCVSL model, in which X and Y control the output values. The circuit certainly requires additional parts to determine X and Y , depending upon which logic function is intended to be realized. The mid-inputs X and Y are either $0V$ or V_{DD} . Therefore, they are in fact binary signals. Whatever logic style is used to generate X and Y must accept ternary input signals, but return a binary one. The performance of the whole circuit depends on the implementation method of these controlling parts.

3. Previous DCVSL Ternary Half Adder

As it is known, a half adder has the same number of inputs (a and b) and outputs (Sum and $Carry$). The outputs represent the numerical addition of the input values (Table 1). A ternary half adder has been presented in [16] by using DCVSL, CTL, and bridge-style circuits. The whole design (Fig. 3) follows the same concept of ternary DCVSL discussed in Section 2. It has three main parts:

1. A part in which the capacitive summation of input variables ($\Sigma_{in}=a+b$) is achieved: It is worth it to mention that the capacitive summation has a linear increase, and it is different from the numerical addition. Two outputs are required to represent the numerical addition when the result is $2+2=4$. Therefore, capacitive summation and numerical addition are not interchangeable at all.

The capacitive summation (Σ_{in}) is generated by two capacitors dividing voltage between a and b (Fig. 3). The truth table of the ternary half adder can be represented alternatively based on the concept of capacitive summation (Table 2). A set of Threshold Detectors (TDs) can distinguish the value of Σ_{in} . They are in fact inverters with properly shifted Voltage Transfer Characteristics (VTC). For example, $TD_{2.5}$ inverts its output value as soon as Σ_{in} increases from 2 to 3 (Tables 3 and 4). The first part of the circuit is in accordance with the basic idea in CTL.

2. The controlling parts which generate X_{Sum} , Y_{Sum} , X_{Carry} , and Y_{Carry} : The initial explanations in Section 2 leads

to the conclusion that the controlling signals X and Y must activate the n-type transistors of the DCVS body whenever their corresponding output is supposed to be '0' or '1' (but not '2'). Thus, according to Tables 3 and 4, the logical expressions are described by Eqs. 1 to 4. X_{Sum} is a 2-input Exclusive-NOR (XNOR) gate, implemented by a regular CMOS structure including 8 transistors (Fig. 4a). Y_{Sum} is a 3-input XNOR, which is implemented by a bridge-style circuit [17, 18] containing 16 transistors (Fig. 4b). Furthermore, X_{Carry} is always in an activating mode since the output carry never becomes '2' in a ternary half adder (Table 4). Thus, X_{Carry} is constantly connected to power supply (Fig. 3).

3. Two ternary DCVS parts which produce the final outputs: As it was explained before, the DCVS structure produces two complementary outputs in parallel. In Fig. 3, $Out1$, $Out2$, $Out3$, and $Out4$ are Sum , \overline{Sum} , $Carry$, and \overline{Carry} , respectively. However, they are not the final outputs yet. Some ternary inverters are also provided with the aim of increasing driving power of the cell. Therefore, the entire design is able to charge and discharge external loads quicker. Eventually, resistors are implemented by n-type and p-type transistors which are constantly switched-on.

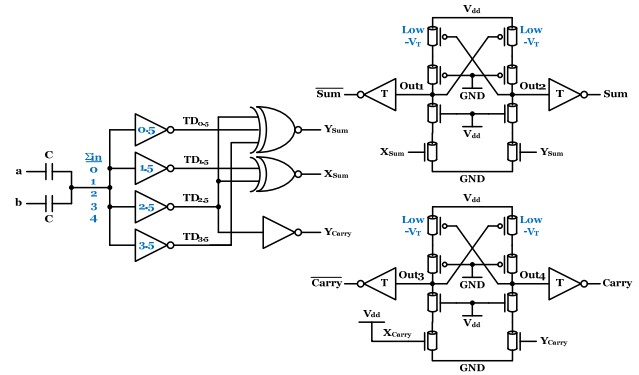


Figure 3: The previous DCVS ternary half adder [16].

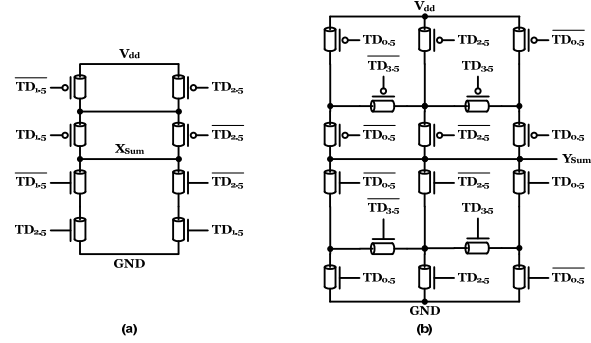


Figure 4: Implementation of XNOR gates [16], (a) 2-input XNOR by CMOS style, (b) 3-input XNOR by bridge style.

Table 1: Truth Table of Ternary Half Adder.

a	b	Carry	Sum
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	0	2
1	2	1	0
2	0	0	2
2	1	1	0
2	2	1	1

Table 2: Truth Table of Ternary Half Adder Based on Capacitive Summation.

$\Sigma_{in} = a+b$	Carry	Sum
0	0	0
1	0	1
2	0	2
3	1	0
4	1	1

$$X_{Sum} = \overline{TD_{1.5} \oplus TD_{2.5}} \quad (1)$$

$$Y_{Sum} = \overline{TD_{0.5} \oplus TD_{2.5} \oplus TD_{3.5}} \quad (2)$$

$$X_{Carry} = 2 \quad (3)$$

$$Y_{Carry} = \overline{TD_{2.5}} \quad (4)$$

4. Proposed DCVS Ternary Half Adder

This paper presents a new DCVS ternary half adder which provides higher performance in comparison with the previous one [16]. DCVS circuits are usually area-consuming since they produce redundant outputs. Transistor reduction is another most important target of this paper. The proposed design has the same CTL and DCVSL parts as well. For the sake of brevity, the similar and repetitive parts will not be explained again, and the main focus will be on the generation of the controlling signals.

As it is clear from Table 3, X_{Sum} and Y_{Sum} are equal to $XNOR(TD_{1.5}, TD_{2.5})$ and $XNOR(TD_{0.5}, TD_{2.5}, TD_{3.5})$, respectively. However, the implementation of XNORs in CMOS and bridge styles requires a high number of transistors. To mention specifically, 30 transistors have been used in [16] to obtain them. An efficient alternative solution is to use pass-transistor logic. Generally, and intrinsically, PTL consumes fewer transistors than the CMOS-like logic styles, owing to the fact that it eliminates one of the networks (PUN or PDN). Table 5 exhibits the followings:

- X_{Sum} equals $TD_{1.5}$ when $TD_{2.5}=2$
- X_{Sum} equals '2' when $TD_{2.5}=0$
- Y_{Sum} equals $TD_{0.5}$ when $TD_{2.5}=2$
- Y_{Sum} equals $TD_{3.5}$ when $TD_{2.5}=0$

There are actually two multiplexers whose selectors are $TD_{2.5}$ (Fig. 5). Although it is possible to choose other threshold detectors as the selector, the selection of $TD_{2.5}$ leads to the least number of transistors. As one can observe in Fig. 5, $TD_{1.5}$ is not required any more. Therefore, not only does PTL lead to fewer transistors, but also one inverter can be eliminated from the previous design.

Table 3: Description of the Controlling Signals X_{Sum} and Y_{Sum} .

Σ_{in}	$TD_{0.5}$	$TD_{1.5}$	$TD_{2.5}$	$TD_{3.5}$	Out1 = Sum	X_{Sum}	Out2 = Sum	Y_{Sum}
0	2	2	2	2	0	2	2	0
1	0	2	2	2	1	2	1	2
2	0	0	2	2	2	0	0	2
3	0	0	0	2	0	2	2	0
4	0	0	0	0	1	2	1	2

Table 4: Description of the Controlling Signals X_{Carry} and Y_{Carry} .

Σ_{in}	$TD_{0.5}$	$TD_{1.5}$	$TD_{2.5}$	$TD_{3.5}$	Out3 = Carry	X_{Carry}	Out4 = Carry	Y_{Carry}
0	2	2	2	2	0	2	2	0
1	0	2	2	2	0	2	2	0
2	0	0	2	2	0	2	2	0
3	0	0	0	2	1	2	1	2
4	0	0	0	0	1	2	1	2

Table 5: An Alternative Description of the Controlling Signals.

$TD_{0.5}$	$TD_{1.5}$	$TD_{2.5}$	$TD_{3.5}$	X_{Sum}	Y_{Sum}
2	2	2	2	2	0
0	2	2	2	2	2
0	0	2	2	0	2
0	0	0	2	2	0
0	0	0	0	2	2

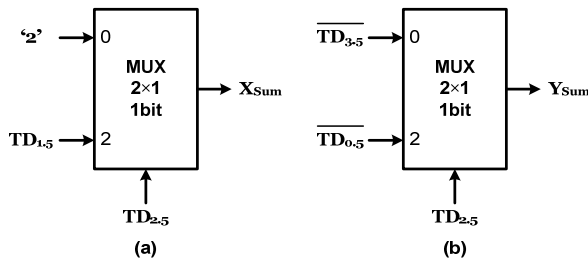

Fig. 5: Schemas for the creation of the controlling signals in the proposed design, (a) X_{Sum} , (b) Y_{Sum} .

Fig. 6 shows the proposed DCVS ternary half adder. It has 63 transistors, 19 fewer transistors than the similar design presented in [16]. In spite of its many advantages, original PTL has two influential defects. Firstly it does not provide full-swing signals since it is often made up of only n-type transistors. Next, it does not restore voltage because it only passes the input signals to the output node. This issue can cause some serious difficulties especially when several PTL circuits are cascaded one after each other. However, the second problem is of no consequence in the proposed design because the PTL parts are isolated inside the cell. Threshold detectors, which are situated before the PTL parts, perform a complete restore.

There are two main solutions to overcome the first problem: *i.* PTL with complementary output, and *ii.* Transmission Gate (TG). Both approaches add more transistors to the circuit.

The latter is utilized in this paper to overcome non-full-swing behavior. TG is an electronic element that selectively blocks or passes a signal level. It is composed of a pair of an n-type and p-type transistors to ensure rail-to-rail operation.

In a MOSFET-like CNFET device [19], one or more carbon nanotubes (CNTs) connect the *source* contact to the *drain* as the channel of transistor. CNTs under the gate terminal are remained intrinsic whereas the end parts joining metallic contacts are doped n^+ with the aim of decreasing schottky barrier effects. The threshold voltage of a CNFET (V_T) is calculated by Eq. 5 [19], where a is the carbon to carbon atom distance, V_π is the carbon π - π bond energy, e is the unit electron charge, and D_{CNT} is the diameter of CNT(s).

$$V_T = \frac{\sqrt{3}a \times V_\pi}{3e \times D_{CNT}} \quad (5)$$

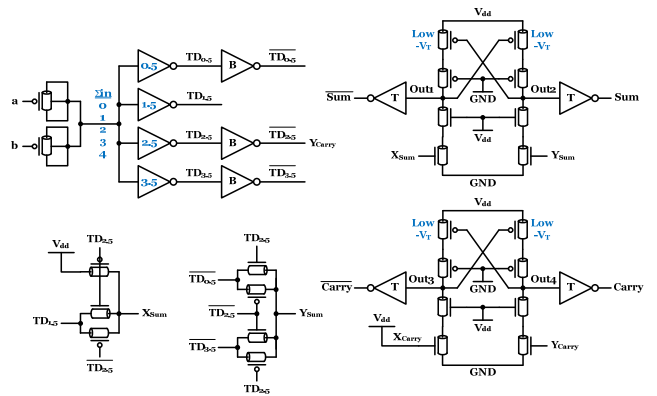


Figure 6: The proposed DCVS ternary half adder.

This paper follows the same transistor sizing explained in [12] for the DCVS part, and the same dimensions for capacitors given in [16]. All of the transistors in the PTL part have three CNTs with the diameter of 1.3311 nanometers. Resistor can be implemented by a constantly switched-on CNFET, whose CNTs resist against flow of charge. In order

to obtain more resistivity, only two CNTs are exploited for these transistors in light of the fact that resistors in parallel reduce resistance. Their *source* and *drain* sides are also lengthened from 32 nanometers to 90 nanometers.

Capacitors can also be implemented by CNFETs, whose *source*, *drain*, and *substrate* are connected together [20]. The junction is one of the capacitor's plates, and the other plate is the gate terminal. The capacitance of a CNFET capacitor is calculated by Eq. 6 [20], where N is the number of CNTs under the gate, C_{CNT} is the capacitance of one CNT, and C_{Gate} is the capacitance proportional to the gate size. As a result, channel length (L_{ch}) and N are increased to 180 nanometers and 500, respectively, for capacitance enlargement. The wider the plates are, the larger the capacitor becomes.

$$C_{CNFET} = N \times C_{CNT} + C_{Gate} \quad (6)$$

5. Simulation Results

Although there are some ternary DCVS circuits in the literature, none of them are adder. To the best of our knowledge, the design presented in [16] is the only DCVS ternary half adder presented so far. Some other state-of-the-art ternary half adders whose structures are also on the basis of capacitive summation are selected in this paper as competitors [5-6]. The last rival is a circuit with a regular design methodology [7]. The entire selection provides a vast range of circuits with different varieties to be able to estimate advantages and disadvantages of the proposed design in comparison with others.

All of the circuits are simulated on HSPICE circuit simulator tool using 32-nanometer CNFET technology [19], [21]. This standard model has been designed for unipolar enhancement-mode MOSFET-like CNFETs where each transistor has one or more CNT(s). It also includes practical non-idealities such as schottky barrier effects, inter-CNT charge screening effects, non-ideal near ballistic transport, back-gate effect, and parasitic resistance and capacitance of *source/drain/gate*. Simulations are performed in three different supply voltages (0.75V, 0.7V, and 0.65V) at room temperature (27°C). In order to provide a realistic output load, fan-out of 4 ternary inverters (TFO4) are used for each output signal [16], [22]. Furthermore, the complete input pattern including 72 transitions are fed to the circuits to obtain maximum delay. Simulation results are shown in Table 6. It displays the most key VLSI evaluating factors, including delay and power consumption. Generally, there is a contradiction between these two parameters. It means that the improvement of one of these factors usually makes the other one deteriorated. Therefore, there is another important parameter, Power-Delay Product (PDP), which makes a balance between them. It is calculated by Eq. 7.

$$PDP = Max(Delay) \times Avg(Power) \quad (7)$$

Table 6: Simulation Results.

Design	Proposed	[16]	[5]	[6]	[7]
V_{DD}			0.75 V		
Delay (ps)	69.666	74.648	88.584	120.57	85.224
Power (μ W)	24.519	24.959	17.238	21.110	17.127
PDP (fJ)	1.7081	1.8632	1.5270	2.5452	1.4596
V_{DD}			0.7 V		
Delay (ps)	74.890	79.982	102.19	111.50	97.642
Power (μ W)	14.641	14.656	8.9608	12.210	8.7981
PDP (fJ)	1.0964	1.1722	0.9157	1.3615	0.8591
V_{DD}			0.65 V		
Delay (ps)	81.498	89.119	103.84	122.57	116.85
Power (μ W)	8.7353	8.7779	4.5787	7.1429	4.2635
PDP (fJ)	0.7119	0.7823	0.4579	0.8755	0.4982

Table 7: Comparison of Outputs Delay in 0.7V Power Supply.

Design	Proposed	[16]	[5]	[6]	[7]
Delay <i>Sum</i> (ps)	74.890	79.982	90.254	111.50	58.067
Delay <i>Sum</i> (ps)	72.691	76.806	102.19	101.75	97.642
Delay <i>Carry</i> (ps)	44.439	46.903	25.853	81.990	47.487
Delay <i>Carry</i> (ps)	56.844	59.328	60.285	41.629	95.282

Simulation results demonstrate that the proposed design is the fastest ternary half adder. DCVS structures benefit from simultaneous generation of an output signal and its inverted version, whereas other structures require additional inverter to do so. This additional inverter causes three major drawbacks:

1. It increases the length of the critical path from the initial inputs to the final output node. This will certainly impose extra delay.

2. It causes asymmetry in the delay of output signals since the inverted version experiences a longer path than the original output. If it is considerable enough, this asymmetry in turn might cause glitches in the proceeding combinational circuits.

3. Any external loads on the first output node are directly situated on the input node of the final inverter. The DCVS circuit must be strong enough to drive external loads as well as the input gate capacitor of the inverter. This will adversely affect the performance of the cell for sure.

Table 7 illustrates the delay parameter for the outputs \overline{Sum} , \overline{Sum} , \overline{Carry} , and \overline{Carry} . The delay gaps between $(\overline{Sum} \& \overline{Sum})$ and $(\overline{Carry} \& \overline{Carry})$ are negligible for the DCVS half adders, whereas the differences are more considerable in other structures.

Despite the fact that DCVSL consumes a lot of power, the proposed half adder has still 19.4% higher performance than [6] in terms of PDP (Table 6). In comparison with the previous DCVS ternary half adder [16], the new version operates with 6.3% higher speed, consumes 0.015 μ W less power, and has 6.4% lower PDP in 0.7V power supply. In addition, it has 19 fewer transistors. Table 8 shows the number of transistors required for the generation of four outputs $(\overline{Sum}, \overline{Sum}, \overline{Carry}, \text{ and } \overline{Carry})$. Also compared to [7], the proposed half adder reduces the number of transistors almost in half.

Eventually, the diameter of CNTs might not be fabricated precisely enough because of the process variations. In order to study the effects of an inaccurate and imperfect chip fabrication, Monte Carlo transient analysis with a reasonable number of 30 iterations for each simulation is performed. Considering fabrication inaccuracies, deviation range from each mean value is from 0.04 to 0.2 nanometers [23]. The maximum amount is taken into account in this paper to test correctness when the worst-case condition is applied. Distribution of diameters is also assumed as Gaussian with 6-sigma distribution. Table 8 shows that DCVS circuits as well as the design presented in [7] function correctly in all of the simulations. The designs of [5] and [6] are prone to faults.

Table 8: Evaluations in Terms of Transistor Count and Process Variation.

Design	Proposed	[16]	[5]	[6]	[7]
No. of Transistors	63	82	40	26	124
No. of Errors in 30 Monte Carlo Simulation Runs	0	0	2	8	0

6. Conclusion

A novel ternary half adder has been presented in this paper. It has been achieved by integrating different logic styles of CTL, PTL, and DCVSL. The combination results in higher speed, less power dissipation, and elimination of 19 transistors in comparison with a similar architecture, which employs other set of logic styles to produce the controlling signals. DCVS structures have their own advantages and disadvantages. Although they usually require a large number of transistors and consume considerable power, they are fast and robust. They produce the inverted output in addition to the original one. Therefore, they benefit from an intrinsic inner redundancy. The proposed design is the fastest circuit amongst different competitors, and is capable of working correctly in the presence of voltage and process variations.

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