The CSI Journal on
Computer Science and Engineering
Vol. 17, No. 2, 2020
Pages 46-61
Regular Paper

Efficient Symmetrical Imprecise 1-Bit Full Adder Cells Using CNFET Technology for Image Processing Applications

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Abstract

Nowadays energy consumption in mobile electronic consumers is a serious concern than ever. These devices exploit digital signal processing (DSP) blocks in their structure to perform multimedia algorithms. Since in most cases the output of these blocks is used for humans with limited vision perception, it is feasible to utilize approximate computation methods to enhance circuit parameters such as latency, power consumption, area, etc. In fact, the circuit parameters are enhanced at the expense of making some outputs imprecise. In this paper using the remarkable benefits of carbon nanotube field effect transistors (CNFETs) along with approximate computing method, two novel imprecise Full Adder cells are presented. Extensive simulations at both application and switching levels confirm the supremacy of the proposed cells against their conventional and state-of-the-art counterparts. Moreover, to study the robustness of the proposed cells against process variations, Monte Carlo transient analysis in the presence of carbon nanotube (CNT) diameter variations is performed. Simulation results indicate the robustness of the proposed cells.

Keywords: Approximate Computing; CNFET, Full Adder, Image Processing.

1. Introduction

Nowadays energy consumption has become an important challenge than ever. According to Moore's law, the number of transistors per unit area of an integrated circuit (IC) doubles almost every 18-24 months [1]. Hence, the growth in the number of transistors will increase the chip's power consumption. On the other hand, the complexity of algorithms is growing very fast. Therefore, the speed of circuits to run algorithms in a reasonable amount of time is also an important figure of merit that should be taken into account. Today there are numerous portable battery-based electronic consumers (i.e. cellular phones, notebooks, laptops, tablets, personal digital assistants (PDAs), etc.) that demand lower power consumption and higher speed. Therefore, the power-delay product (PDP) metric makes a compromise between power consumption and delay of circuits [2].

Improvement of circuit parameters can be done at three levels of technology, logic design, and computation method [3]. At the technology level, we utilize carbon nanotube field effect transistors (CNFETs) because of their unique features such as the near ballistic operation of CNFETs and one-dimensional band structure [4]. At the logic level, we utilize transmission gate logic (TGL) [5] and also pass transistor logic (PTL) [6] to reduce transistor count. At the computation level, we deploy an approximate method to relax some outputs to achieve higher performance [7].

Limited perception of human vision is a good opportunity to design inexact circuits with the aim of improving circuit parameters. At approximate computation, some outputs are relaxed. In other words, there are erroneous outputs for some combinations of inputs. This technique can be used in applications that are tolerable in presence of error. Digital signal processors (DSPs) including image, audio, or video blocks can apply approximate computation methods at the expense of losing exactness. Ultimately, it is desirable to have a balance between energy consumption and accuracy. In this paper, we take into account the product of PDP and accuracy to make a tradeoff between them.

Full Adder cell is the building block of DSP cores. It is used to construct larger arithmetic circuits such as subtractor, multiplier, compressor, divider, etc. They in turn are used to realize digital signal processing applications. It is evident that efficient design of a 1-bit Full Adder cell can affect the performance of the entire digital system. From the above, it is an indispensable task to design high-performance Full Adder cells [8].

In this paper, we present two novel CNFET-based imprecise Full Adder cells using TGL and PTL logics. The proposed cells deploy inverter gates at the output stage which reinforce their driving capability in the presence of large loads. To evaluate their efficiency comprehensive simulations are conducted at two abstraction levels including application and switching level. At the application level, we use a motion detector which is one of the applications of image processing [9, 10]. At the switching level, we conduct comprehensive simulations with regard to power supply, output load, and temperature variations. Also, we study the robustness of the proposed cells against process variations using *Monte Carlo* transient analysis. All simulations indicate the efficacy of the proposed cells.

The remainder of this manuscript is structured as follows. Section 2 includes a brief review of concepts of approximate computing and characteristics of CNFET technology. Section 3 represents a review of previous work about inexact Full Adder cells addressed in the literature. The novel proposed Full Adder cells are described in detail in Section 4. Section 5 includes simulation results and comparisons. Finally, Section 6 concludes the paper.

2. Preliminary Concepts

2.1. Approximate Computing

Approximate computing is a fruitful method to improve circuit parameters such as power consumption, delay, and area through relaxing the outputs of the circuit for some inputs [11]. In other words, it produces some erroneous outputs for a number of input combinations. This method leads to a reduction in the complexity of circuits and consequently increases the performance of the circuit. Approximate computing can be applied in applications that are tolerant against errors. Digital signal processing (i.e. image, audio, or video processing), pattern recognition, computer vision, machine learning, web-based search, multimedia, big data analysis, and MapReduce are some of these applications [12].

Various new metrics have been proposed to evaluate the reliability of inexact circuits in [13]. Two of the most important metrics are mean error distance (MED) and normalized error distance (NED) that can be calculated by sequential probability transition matrices (SPTMs). The MED considers the average effect of different inputs on the outputs. On the other hand, the NED which is not dependent on the size of operands evaluates the reliability of adders. The MED and NED metrics are computed using Eqs. 1 and 2, respectively [13].

$$MED = \sum_i d_i \times q_i \qquad (1)$$

$$NED = \frac{MED}{D} \qquad (2)$$

Where d_i denotes the error distance (ED) computed using the arithmetic distance between exact (i.e., golden) and inexact output for the *i*th sequence of input fed to the circuit,

q_i denotes the probability of occurrence of *i*th input pattern and *D* denotes the maximum value of error that an inexact circuit can produce. For instance, if *n* lower bits are inexact, then *D* is 2^n.

2.2. Carbon Nanotube Field Effect Transistor (CNFET)

Carbon nanotube (CNT) was discovered by S. Iijima in 1991 [14]. The CNTs are consisting of rolling sheets of graphite. They are divided into two different classes called single-walled carbon nanotube (SWCNT) and multi-walled carbon nanotube (MWCNT). In SWCNT there is only one cylinder while in MWCNT there is more than one cylinder nested inside each other [8]. In MWCNT, the distance between two adjacent CNTsise 0.34nm [15]. The SWCNT is categorized into three different classes called zigzag, armchai,r and chiral according to chirality vector which is determined by (n_1, n_2) indices. Als,o a SWCNT is metallic if $|n_1\text{-}n_2|=3K$ ($K \in \mathbb{Z}$) or $n_1=n_2$ and otherwise it is semiconducting. As shown in Fig. 1, CNTs are used as the channel of CNFETs [3]. The distance between the centers of two adjacent CNTs is called pitch.

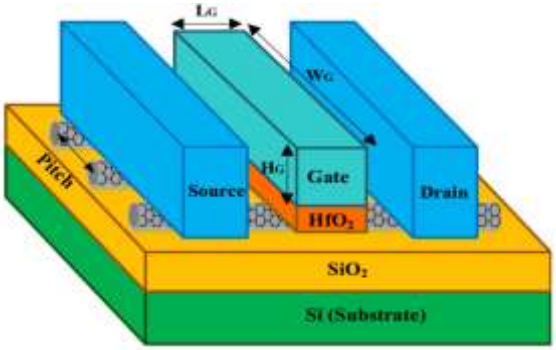


Fig. 1. 3-D view of CNFET

Like silicon-bulk transistors, the CNFETs require the threshold voltage (V_{th}) to be turned on as well. The threshold voltage has an inverse relation with the diameter of the CNT. The threshold voltage is calculated using Eq. 3 [16].

$$V_{th} = \frac{\sqrt{3}}{3} \times \frac{a \times V_\pi}{e \times D_{CNT}} \cong \frac{0.43}{D_{CNT(nm)}} (V) \qquad (3)$$

Where a (0.249 nm) is the CNT lattice constant, V_π is the carbon π–π bond energy in the tight bonding model (≃3.033 *e*V), e is the unit electron charge and D_{CNT} is the diameter of carbon nanotube which is computed using Eq. 4 [16].

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \cong 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad (4)$$

The CNFETs are divided into three different types addressed in the literature, i.e., SB-CNFET, MOSFET-like CNFET, and T-CNFET [17]. The first type operates on the basis of direct tunneling through a Schottky barrier (SB) at the source-channel junction. The SB-CNFET is manufactured by using direct junction of carbon nanotubes with metal which leads to forming SB at the metal-channel junction. The SB-CNFET has two major handicaps. First, the SB restricts the device current in the ON state which reduces its performance. Second, SB results in an ambipolar attitude that limits its usage in the CMOS logic family.

Due to constraints on SB-CNFETs, attempts have been made to construct transistors that operate in accordance with the CMOS family [18, 19]. In MOSFET-like devices, source and drain regions are heavily doped with potassium. Numerical studies which have been done in [19] indicate that MOSFET-like devices show unipolar characteristics. Also because of lacking SB at the source-channel junction, they have higher ON current and they are suitable for high-performance applications.

The third type which is called band-to-band tunneling CNFET (T-CNFET) is composed of source and drain regions doped with p^+ and n^+, respectively [20]. The T-CNFET has super cutoff characteristics and low ON current which makes it to be suitable for ultra-low-power applications.

In this paper, considering the advantages and disadvantages of each type of transistors mentioned above, the high-performance MOSFET-like CNFET is used to design inexact Full Adder cells.

3. Previous Work

In this section, we will briefly review features of inexact Full Adder cells addressed in the literature. In fact, we will investigate their functionality parameters at the application

level such as MED and NED, and also circuit level parameters such as transistor count, critical path, and driving capability.

The structure of the NAND_NOR Inexact Full Adder (NNIFA) is illustrated in Fig. 2 [10]. It consists of 12 transistors that 4 of them are placed on the critical path of the cell. The main obstacle of NNIFA design is that its *SUM* signal does not provide rail-to-rail outputs. Therefore, it has no driving capability and will encounter difficulty within larger arithmetic circuits. The MED and NED metrics for the NNIFA cell are calculated in Eqs. 5 and 6, respectively.

$$MED = \frac{1}{8} \times [1 + 0 + 0 + 0 + 0 + 0 + 0 + 1] = 0.25 \quad (5)$$

$$NED = \frac{0.25}{3} = 0.08333 \quad (6)$$

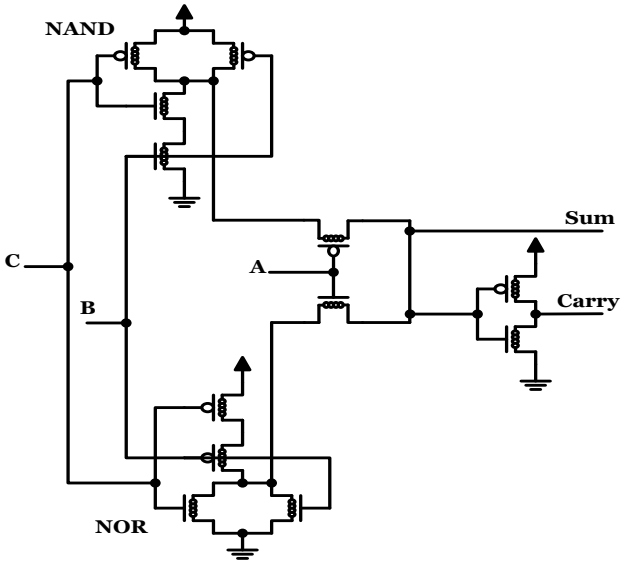


Fig. 2. The design of NNIFA

The structure of transmission gate based designs namely TGA1 and TGA2 are shown in Fig. 3 [21]. The TGA1 and TGA2 designs are composed of 16 and 22 transistors, respectively. Moreover, the critical path of both designs contains 5 transistors which lead to large propagation delay. From the point of view of the driving ability, the output carry (i.e., *Cout*) signal in TGA1 has weak functionality in the presence of large loads, since it is not full swing. On the other hand, the TGA2 design provides rail-to-rail output signals which are proper for large loads. The MED and NED metrics for both TGA1 and TGA2 designs are 0.25 and 0.08333, respectively.

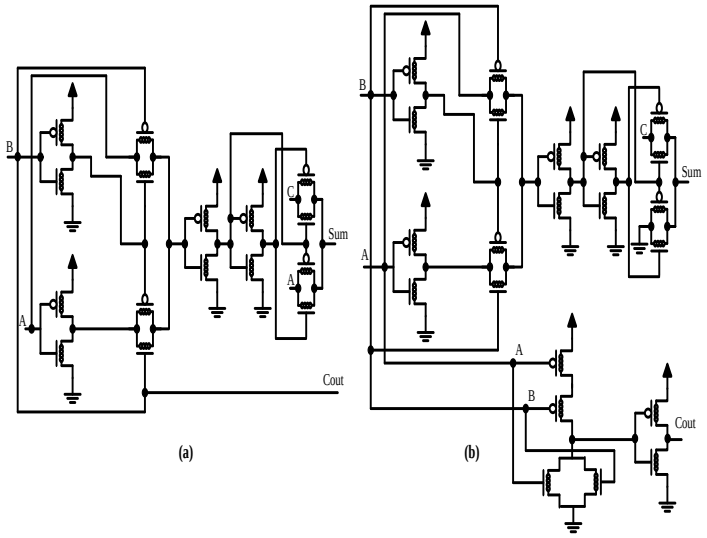


Fig. 3. Transmission gate based designs (a) TGA1 (b) TGA2

The structure of XOR/XNOR based inexact Full Adders called AXA1 and AXA2 are shown in Fig. 4 [22]. The AXA1 and AXA2 designs consist of 8 and 6 transistors, respectively. The critical path of AXA1 and AXA2 cells consist of 4 and 3 transistors, respectively. The AXA2 design suffers from lacking driving capability due to having threshold loss problem at the output nodes by V_{dd}-$2V_{th}$. Therefore AXA2 will have malfunction against large loads. However, its critical path is shorter than AXA1 by one transistor. The MED and NED parameters for both AXA1 and AXA2 designs are 0.5 and 0.16666, respectively.

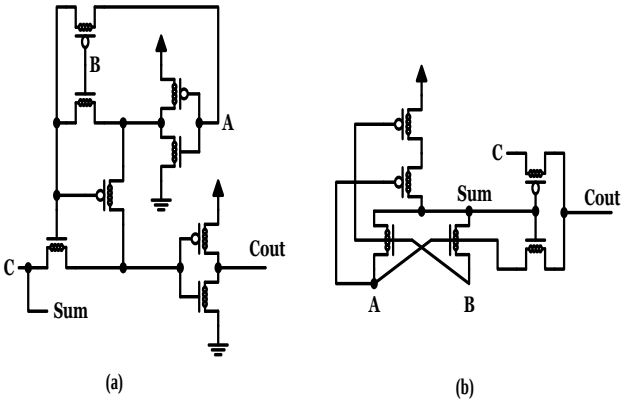


Fig. 4. XOR/XNOR based designs (a) AXA1 (b) AXA2

Figure 5 indicates the structure of InXA1 and InXA2 designs which are based on XOR logic [23]. As shown in Fig. 5 the InXA1 has 8 transistors while the InXA2 contains 10

transistors. The critical paths of InXA1 and InXA2 consist of 3 and 4 transistors, respectively. These designs provide non-full swing outputs which reduce their driving ability, especially in the presence of large loads. At both designs, the *SUM* signal will be V_{dd}-$2V_{th}$ for some combinations of inputs which is far from being full swing. The MED parameter for InXA1 and InXA2 are 0.5 and 0.25, respectively. Consequently, the NED parameter is 0.16666 and 0.08333, respectively.

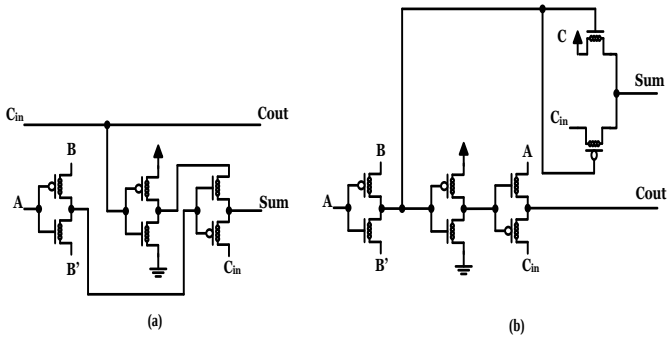


Fig. 5. Inexact Full Adders based on XOR logic (a) InXA1 (b) InXA2

4. Proposed Work

The truth table of the proposed inexact Full Adder cell is tabulated in Table 1. The entries marked with the symbol 'x' indicate fallacious values. In the proposed design the *Cout* signal is incorrect only in one case while the *SUM* signal is incorrect in three cases out of eight possible combinations of inputs as shown in Table 1. In the following, we will present two inexact Full Adder cells based on transmission gate and pass transistor logics.

Table 1. Truth table of the proposed inexact Full Adder cell

Input			Exact			Inexact			
A	B	C	NOR (A,B)	C_{out}	SUM	C_{out}	SUM	$\overline{C_{out}}$	$\overline{SUM}$
0	0	0	1	0	0	0	1x	1	0x
0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	0	1	1	0
0	1	1	0	1	0	1	0	0	1
1	0	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	0	0	1
1	1	0	0	1	0	0x	1x	1x	0x
1	1	1	0	1	1	1	0x	0	1x

If we take a look at Table 1 it is evident that the $\overline{SUM}$ signal can be realized using Eq. 7. First, the NOR function is computed using input signals *A* and *B*. Then it is used as the select line of a 2x1 multiplexer to produce the $\overline{SUM}$ signal. Now by applying an inverter gate at the output stage we can produce *SUM* output. The existence of an inverter gate at the output stage is an affirmative point because results in increasing the driving capability of the *SUM* signal.

$$\overline{SUM} = \overline{\overline{(A+B)}}.C + \overline{(A+B)}.0 \quad (7)$$

If we consider Table 1 again, we can implement the *Cout* signal by using Eq. 7. In fact, when the output of the NOR function is equal to logic '1' then the *Cout* signal is logic '0' and otherwise, it is equal to the value of input *C*. The first design called 14TIFA1 is shown in Fig. 6 at the transistor level. Therefore, as depicted within the colored box in Fig. 6, there is a fully symmetric circuit for realizing both outputs, i.e. *SUM* and *Cout*. This feature eases creating layout process of the circuit. Another advantage of the proposed design is that all internal and output nodes are full swing. The critical path of 14TIFA1 cell belongs to the *SUM* signal with 5 transistors. According to Table 1, the MED and NED parameters are 0.375 and 0.125, respectively.

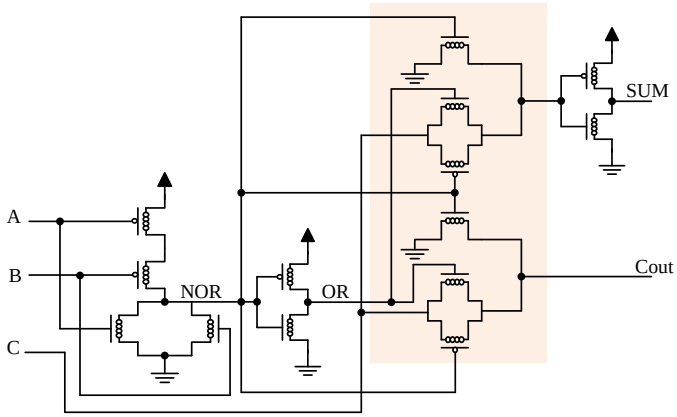


Fig. 6. The structure of the proposed 14TIFA1 design

The second design which is called 14TIFA2 is shown in Fig. 7. Unlike the 14TIFA1 design, both the *SUM* and *Cout* signals are produced using inverter gates which increase driving capability. The 14TIFA2 uses pass transistor logic (PTL) to realize output signals. As shown in the colored box in Fig. 7, the 14TIFA2 deploys symmetric circuits to produce

SUM and *Cout* outputs which facilitate creating the layout process. The critical path which belongs to the *Cout* signal consists of four transistors which is one transistor less than 14TIFA1. Therefore, the 14TIFA2 design has a smaller delay than 14TIFA1. The MED and NED parameters are the same as 14TIFA1 due to having similar truth tables.

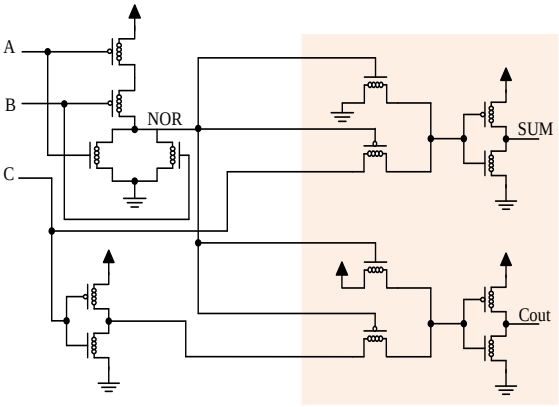


Fig. 7. The structure of the proposed 14TIFA2 design

5. Simulations and Discussion

5.1. Application

To evaluate the efficacy of the proposed cells in terms of peak signal-to-noise ratio (PSNR) we have carried out computer simulations using the MATLAB tool. In fact, we use the motion detector application in image processing to evaluate the PSNR metric for each inexact Full Adder cell [9, 10]. So the higher PSNR value indicates the higher efficiency of the Full Adder cell.

In this application, there are two frames namely Q_1 and Q_2 to be subtracted from each other pixel by pixel. If there is no movement then the difference is equal to zero. In image processing, a zero pixel produces a dark point in the picture. Therefore, in case of not having movement (i.e. Q_1=Q_2) we observe a dark image as output, otherwise, there will be shadows. Each pixel is composed of 8 bits. To subtract two 8-bit binary digits we apply 2's complement method. First, we obtain the 2's complement of the subtrahend and then add it to the minuend. It is worth noting that in image processing there is no negative number and each pixel is in the range of 0 to 255. We use an 8-bit ripple carry adder (RCA) which consists of four inexact Full Adder cells at least significant bits while the higher significant bits remain exact. If the difference is negative it is rounded to zero value. Frames Q_1 and Q_2 which are minuend and subtrahend are illustrated in Fig. 8.

(a) (b)

Fig. 8. Input frames for motion detector (a) Q1 (b) Q2

The PSNR metric which determines the quality of the picture is calculated using Eq. 8 [25]. The parameter MAX_f demonstrates the maximum value of the signal existing in the image and the e_{MSE} shows the mean squared error.

$$PSNR = 10\log_{10}\frac{MAX_f^2}{e_{MSE}} \quad (8)$$

The e_{MSE} parameter is calculated using Eq. 9. Symbols *m* and *n* represent the numbers of rows and columns existing in an image.

$$e_{MSE} = \frac{1}{mn}\sum_{i=1}^{m}\sum_{j=1}^{n}[Q_1(i,j) - Q_2(i,j)]^2 \quad (9)$$

The simulation results for the subtraction of Q_1 and Q_2 frames with inexact Full Adders and exact ones are shown in Fig. 9. Performing subtraction with inexact cells may produce shadows in the resultant picture even if there is no movement in the initial pictures. However, if the subtraction error is low, these noises are hardly understood by humans.

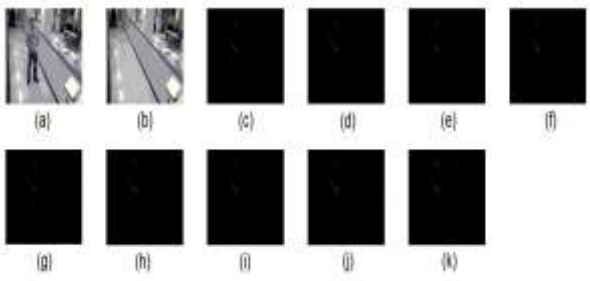


Fig. 9. Subtraction results (a) Q1 (b) Q2 (c) exact adder (d) proposed adder (e) NNIFA (f) TGA1 (g) TGA2 (h) AXA1 (i) AXA2 (j) InXA1 (k) InXA2

The PSNR parameters obtained from the motion detector application are tabulated in Table 2. The PSNR value for both

proposed designs is 37.9441dB. According to Table 2, the highest PSNR belongs to the TGA1 cell following with NNIFA, the proposed 14TIFA cells, AXA1, TGA2, AXA2, InXA2, and InXA1. Quantitative results confirm that there is a close competition between the proposed cells and previous ones in terms of PSNR figure of merit.

Table 2. PSNR results for motion detector application

Design	Reference	PSNR(dB)
14TIFA1	Proposed	37.9441
14TIFA2	Proposed	37.9441
NNIFA	[10]	37.9986
TGA1	[21]	42.0027
TGA2	[21]	37.8283
AXA1	[22]	37.8656
AXA2	[22]	35.7634
InXA1	[23]	34.3711
InXA2	[23]	34.9356

5.2. Switching Level

In this section, we carry out simulations at the switching level to evaluate hardware parameters such as power consumption, delay, and PDP as well as the product of PDP by transistor count and PSNR values to tradeoff between all of them. In fact, all cells are simulated under different conditions such as power supply, output load, and ambient temperature variations. Finally, the robustness of the proposed cells is scrutinized against diameter deviations of CNTs by using *Monte Carlo* transient analysis.

We use compact SPICE model for CNFETs with 32nm feature size developed at Stanford University [26, 27]. This model supports unipolar MOSFET-like transistors that each CNFET can have one or more CNTs as its channel. This model takes into account non idealities including Schottky barrier effects, parasitics, including CNT, source/drain, and gate resistances and capacitances, and CNT charge screening effects. Table 3 tabulates some of the important parameters existing in this model.

Table 3. Some CNFET parameters [26, 27]

Parameter	Value	Description
L_{ch}	32nm	Physical channel length
L_{geff}	100nm	The mean free path in the intrinsic CNT channel
L_{ss}	32nm	The length of doped CNT source-side extension region
L_{dd}	32nm	The length of doped CNT drain-side extension region
K_{gate}	16	The dielectric constant of high-K top gate dielectric material
T_{ox}	4nm	The thickness of high-K top gate dielectric material
C_{sub}	40pF/m	The coupling capacitance between the channel region and the substrate
Efi	0.6ev	The Fermi level of the doped S/D tube

In our simulations, transistor sizes are as follows. The parameter n_1 is 19 except for those that have threshold loss problems in which cases it is set to 73 to mitigate it. If n_1 is equal to 19 and 73 then the threshold voltage would be 0.28V and 0.07V, respectively. Moreover, the number of tubes for all transistors is set to 3.

The simulation environment is depicted in Fig. 10. To have realistic inputs we apply buffers at the input stage [2]. Also, we use loads at the output stage. Complete test pattern which includes 56 combinations of inputs is fed to the circuit under test. To evaluate the delay metric, we separately calculate the delay of *SUM* and *Cout* signals and consider the maximum one to report it as the delay of the circuit. The delay is calculated from the moment that the input signal reaches its 50% of maximum value until the output signal reaches the same voltage level. Delay is considered for the rise and fall of each output signal and finally, the maximum one is reported in this paper.

Power consumption is the average power that is measured during the long time of simulation. The PDP is another metric that compromises between power and delay of circuits. Moreover, to make a tradeoff between PDP, area, and

accuracy of circuits we consider two more metrics called power-delay-area product (PDAP) and power-delay-area-PSNR product (PDAPP). By PDAP and PDAPP metrics we can better determine the supremacy of inexact circuits because of making a tradeoff between all parameters. We already know that the goal of an inexact circuit is to enhance hardware parameters at the expense of losing accuracy as much as possible. However, that does not mean we reduce the accuracy to the desired extent to improve hardware parameters. In other words, we have to make a compromise between all criteria, because of the limitation in the reduction of the accuracy. So we can compare and criticize different circuits in a fair condition by PDAP and PDAPP metrics.

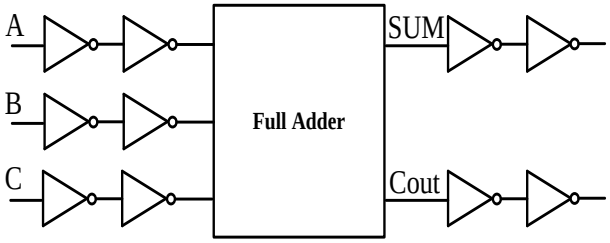


Fig. 10. Simulation environment

First, we study the efficiency of inexact Full Adders under variant power supplies ranging from 0.8V to 1.1V at room temperature (25°C) and 1GHz operating frequency. Simulation results are listed in Table 4. At 0.8V power supply, the lowest PDAP and PDAPP belong to InXA2 due to having lower power consumption compared to other cells. However, the proposed 14TIFA2 circuit has very close results to the InXA2 circuit at 0.8V V_{dd}. But in other power supplies, the proposed 14TIFA2 outperforms other circuits in terms of PDAP and PDAPP metrics. Meanwhile, its delay is better than previous ones and it provides reasonable power consumption as well. For instance at 0.9V power supply the delay of 14TIFA2 is about 25%, 72%, 35%, 0.7%, 39%, 74%, 42% and 52% less than 14TIFA1, NNIFA, TGA1, TGA2, AXA1, AXA2, InXA1 and InXA2, respectively. Again at the same voltage level the proposed 14TIFA2 offers better PDAPP nearly 24%, 69%, 46%, 22%, 8%, 48%, 14% and 25% in comparison with 14TIFA1, NNIFA, TGA1, TGA2, AXA1, AXA2, InXA1 and InXA2, respectively. Considering Table 4 it is apparent that the lowest delay belongs to the proposed 14TIFA2 inexact design at 0.8V and 0.9V power supplies and its amount of power consumption is competitive to other cells. Also in terms of transistor count, it has a smaller number of transistors compared to TGA1 and TGA2 designs. Based on the results listed in Table 4 the proposed cells overcome other ones when considering all hardware and application parameters altogether.

Table 4. Simulation results versus power supply variations

Design	Power (10^{-6} W)	Delay (10^{-12} S)	PDP (10^{-17} J)	No. Tr.	PDAP (10^{-17} J)	1/PSNR (1/dB)	PDAPP (10^{-17} J/dB)
Vdd=0.8V							
14TIFA1	5.8674	148.34	87.040	14	1218.56	0.02635	32.1090
14TIFA2	5.9317	111.04	65.868	14	922.152	0.02635	24.2987
NNIFA	6.0932	413.85	252.16	12	3025.92	0.02631	79.6119
TGA1	6.8014	177.58	120.78	16	1932.48	0.02380	45.9930
TGA2	4.8525	117.14	56.843	22	1250.54	0.02643	33.0517
AXA1	6.8062	187.70	127.75	8	1022	0.02640	26.9808
AXA2	6.3868	465.04	297.01	6	1782.06	0.02796	49.8263
InXA1	6.2239	191.34	119.09	8	952.72	0.02909	27.7146
InXA2	4.8057	159.10	76.459	10	**764.59**	0.02862	**21.8825**

Vdd=0.9V							
14 TIFA 1	7.527 1	1 33.51	1 00.50	14	14 07	0.0263 5	37 .074 4
14 TIFA 2	7.578 6	1 00.05	7 5.826	14	**10 61.56**	0.0263 5	**27 .9721**
N NIFA	7.939 2	3 63.32	2 88.45	12	34 61.4	0.0263 1	91 .069 4
T GA1	8.792 2	1 56.04	1 37.19	16	21 95.04	0.0238 0	52 .241 9
T GA2	6.187 8	1 00.79	6 2.365	22	13 72.03	0.0264 3	36 .262 7
A XA1	8.688 6	1 66.66	1 44.81	8	11 58.48	0.0264 0	30 .583 8
A XA2	8.231 6	3 92.17	3 22.82	6	19 36.92	0.0279 6	54 .156 2
In XA1	8.069 0	1 74.10	1 40.49	8	11 23.92	0.0290 9	32 .694 8
In XA2	6.242 1	2 09.38	1 30.70	10	13 07	0.0286 2	37 .406 3
Vdd=1V							
14 TIFA 1	9.390 3	1 25.69	1 18.02	14	16 52.28	0.0263 5	43 .537 5
14 TIFA 2	9.421 8	9 2.924	8 7.552	14	**12 25.72**	0.0263 5	**32 .2977**
N NIFA	10.089	3 32.65	3 35.60	12	40 27.2	0.0263 1	10 5.955
T GA1	11.112	1 41.92	1 57.70	16	25 23.2	0.0238 0	60 .052 1
T GA2	7.763 8	9 0.657	7 0.385	22	15 48.47	0.0264 3	40 .926 0
A XA1	10.846	1 54.38	1 67.44	8	13 39.52	0.0264 0	35 .363 3
A XA2	10.380	3 40.54	3 53.49	6	21 20.94	0.0279 6	59 .301 4
In XA1	10.174	1 62.79	1 65.63	8	13 25.04	0.0290 9	38 .545 4
In XA2	7.934 2	2 06.01	1 63.45	10	16 34.5	0.0286 2	46 .779 3
Vdd=1.1V							
14 TIFA 1	11.528	1 19.29	1 37.52	14	19 25.28	0.0263 5	50 .731 1
14 TIFA 2	11.533	8 7.100	1 00.45	14	**14 06.3**	0.0263 5	**37 .0560**
N NIFA	12.504	3 08.34	3 85.54	12	46 26.48	0.0263 1	12 1.722
T GA1	13.730	1 30.08	1 78.60	16	28 57.6	0.0238 0	68 .010 8
T GA2	9.499 8	8 3.813	7 9.621	22	17 51.66	0.0264 3	46 .296 3
A XA1	13.263	1 45.44	1 92.89	8	15 43.12	0.0264 0	40 .738 3
A XA2	12.802	2 99.61	3 83.54	6	23 01.24	0.0279 6	64 .342 6
In XA1	12.533	1 56.14	1 95.68	8	15 65.44	0.0290 9	45 .538 6

InXA2	9.7772	193.72	189.41	10	1894.1	0.02862	54.2091

Driving capability is one of the important features of a circuit that should be taken into account. In this regard, we study the driving capability of cells in presence of variant output loads ranging from 5fF to 20fF at 0.9V power supply, room temperature, and 1GHz operating frequency. Results obtained from simulations are listed in Table 5. Computer simulations confirm the superiority of the proposed 14TIFA2 cell at all loads except for 5fF in terms of the PDAPP parameter. For instance, If we take into account the PDAPP parameter at a load of 15fF it is evident that the proposed 14TIFA2 design outperforms other cells by about 27%, 47%, 25%, 15%, 48%, 19% and 18% in comparison with 14TIFA1, TGA1, TGA2, AXA1, AXA2, InXA1 and InXA2, respectively. It is worth mentioning that the NNIFA cell fails to work at 15fF and 20fF loads. If we consider more parameters altogether such as PDAP and PDAPP it is apparent that the proposed cells function better than others do. Simulations at larger loads such as 20fF indicate that AXA2 cell fail to function due to lacking enough driving capability. While the proposed cells not only perform reasonable operations but also they even extend their distance from other circuits in some cases in terms of PDAP and PDAPP metrics due to enjoying inverter gates at the output stages. For instance at 20fF load the 14TIFA2 outperforms 14TIFA1, TGA1, TGA2, AXA1, InXA1 and InXA2 in terms of PDAPP by about 26%, 47%, 25%, 18%, 21% and 15%, respectively.

Table 5. Simulation results in presence of variant output loads

Design	Power (10^{-6} W)	Delay (10^{-12} S)	PDP (10^{-17} J)	No. Tr.	PDAP (10^{-17} J)	1/PSNR (1/dB)	PDAPP (10^{-17} J/dB)
Cload=5fF							
14TIFA1	4.0364	71.368	28.807	14	403.298	0.02635	10.6269
14TIFA2	4.0336	57.372	23.141	14	323.974	0.02635	8.53671
NNIFA	4.3219	188.35	81.402	12	976.824	0.02631	25.7002
TGA1	4.7865	84.292	40.346	16	645.536	0.02380	15.3637
TGA2	3.3943	54.472	18.489	22	406.758	0.02643	10.7506
AXA1	4.6435	87.005	40.401	8	323.208	0.02640	**8.53269**
AXA2	4.6026	200.18	92.134	6	552.804	0.02796	15.4563
InXA1	4.4201	89.440	39.533	8	**316.264**	0.02909	9.20011
InXA2	3.5843	93.855	33.640	10	336.40	0.02862	9.62776
Cload=10fF							
14TIFA1	7.5271	133.51	100.50	14	1407	0.02635	37.0744
14TIFA2	7.5786	100.05	75.826	14	**1061.56**	0.02635	**27.9721**
NNIFA	7.9293	365.99	290.20	12	3482.4	0.02631	91.6219
TGA1	8.7922	156.04	137.19	16	2195.04	0.02380	52.2419

TGA2	6.1878	100.79	62.365	22	1372.03	0.02643	36.2627
AXA1	8.6886	166.66	144.81	8	1158.48	0.02640	30.5838
AXA2	8.2316	392.17	322.82	6	1936.92	0.02796	54.1562
InXA1	8.0690	174.10	140.49	8	1123.92	0.02909	32.6948
InXA2	6.2421	209.38	130.70	10	1307	0.02862	37.4063
Cload=15fF							
14TIFA1	10.581	196.83	208.27	14	2915.78	0.02635	76.8308
14TIFA2	10.912	139.17	151.86	14	**2126.04**	0.02635	**56.0211**
NNIFA	Failed	Failed	Failed	12	Failed	0.02631	Failed
TGA1	12.424	227.09	282.14	16	4514.24	0.02380	107.438
TGA2	8.7757	146.43	128.50	22	2827	0.02643	74.7176
AXA1	12.665	247.41	313.34	8	2506.72	0.02640	66.1774
AXA2	11.024	590.73	651.22	6	3907.32	0.02796	109.248
InXA1	11.448	260.18	297.87	8	2382.96	0.02909	69.3203
InXA2	8.5787	280.96	241.02	10	2410.2	0.02862	68.9799
Cload=20fF							
14TIFA1	13.028	259.49	338.07	14	4732.98	0.02635	124.714
14TIFA2	13.816	179.65	248.20	14	**3474.8**	0.02635	**91.5609**
NNIFA	Failed	Failed	Failed	12	Failed	0.02631	Failed
TGA1	15.635	295.63	462.22	16	7395.52	0.02380	176.013
TGA2	10.967	192.92	211.58	22	4654.76	0.02643	123.025
AXA1	16.385	325.59	533.47	8	4267.76	0.02640	112.668
AXA2	Failed	Failed	Failed	6	Failed	0.02796	Failed
InXA1	14.470	344.21	498.07	8	3984.56	0.02909	115.910
InXA2	10.603	358.26	379.86	10	3798.6	0.02862	108.715

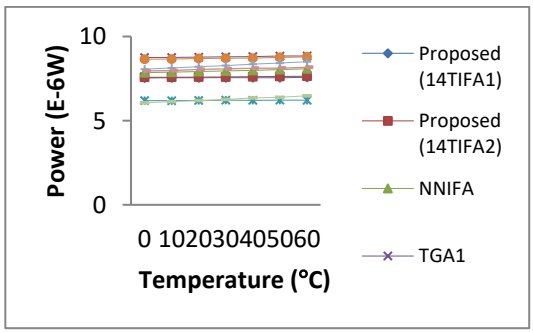
Evaluating the susceptibility of circuits against ambient temperatures is another concern should be studied. For this purpose, we conduct simulations with regard to variant temperatures ranged from 0°C to 60°C at 0.9V power supply and 1GHz operating frequency. Simulation results are shown in Fig. 11.

As shown in Fig. 11 (a), from the power consumption point of view the InXA2 and TGA2 have the lowest power and there is close competition between them. On the other hand, the TGA1 and AXA1 have the highest power consumption,

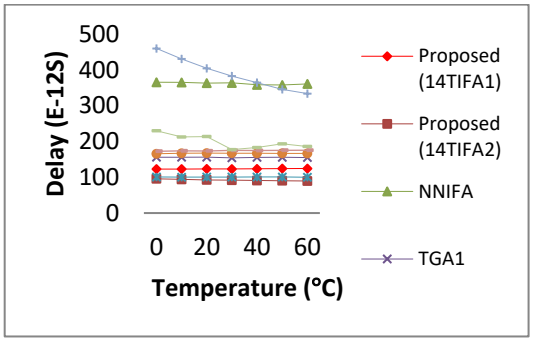
respectively. The reason for the high power consumption is that not only internal nodes are not full swing and lead to having static power consumption but also inputs are directly connected to the outputs that lead to low driving capability. Non full swing internal nodes that have incomplete voltages lead to transistors do not completely switch ON or OFF and there will be current drawn from V_{dd} to ground. Fig. 11 (a) indicates that the proposed cells have lower power consumptions after InXA2 and TGA2 cells.

Variations of delay parameter against different ambient temperatures are shown in Fig. 11 (b). The 14TIFA2, TGA2, and 14TIFA1 have a shorter delay, respectively, than others as shown in Fig. 11 (b). On the other hand, the AXA2 and NNIFA have the highest delays which are not suitable for high-performance applications followed by the TGA1, AXA1, InXA1, and InXA2, respectively. This simulation confirms that the proposed cells are very fast compared to their counterparts.

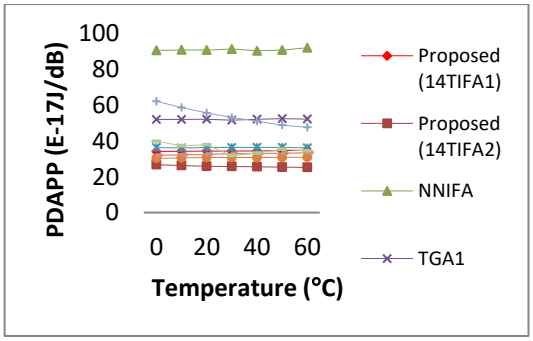
To make a tradeoff between all parameters we consider the PDAPP metric in Fig. 11 (c). The results of PDAPP in this figure clearly show that the proposed 14TIFA2 design is superior to other ones. For instance the proposed 14TIFA2 design outperforms other designs at 60°C by about 27%, 72%, 51%, 30%, 18%, 47%, 24% and 26% in comparison with 14TIFA1, NNIFA, TGA1, TGA2, AXA1, AXA2, InXA1 and InXA2, respectively. Moreover, the worst results belong to NNIFA, TGA1, and AXA2, respectively.



(a)



(b)



(c)

Fig. 11. Performance against temperature (a) Power (b) Delay (c) PDAPP

Since the performance of CNFETs is more sensitive to diameter deviations of CNTs, we study the robustness of the proposed Full Adders against diameter variations by performing transient *Monte Carlo* (*MC*) analysis [28]. Diameter variations of CNTs will alter the threshold voltage of CNFETs and consequently will negatively affect their performance. The *Monte Carlo* analysis with 30 iterations for each simulation is carried out. The statistical significance of 30 iterations is very high [6, 29]. If the circuit under test performs correctly for 30 iterations, then there is 99% probability that more than 80% of the components of the circuit will function properly [24]. We assume a *Gaussian* function for diameter deviations of CNTs with a distribution of 6-Sigma [30]. A standard deviation from the mean in the range of 0.05–0.2nm is considered for each mean diameter value for inspecting the impact of process variation on the robustness of the proposed circuits [24]. Simulation results are tabulated in Table 6. As depicted in Table 6 both the proposed designs perform well against process variations and keep their correct functionality.

Table 6. Parameter variations of the proposed cells against process variations

14TIFA1				
Diameter Deviations (*nm*)	0.05	0.10	0.15	0.20
Delay Variation (E-11)	0.573	1.095	1.723	2.212
Power Variation (E-6)	0.018	0.024	0.035	0.046
PDP Variation (E-16)	0.400	0.771	1.203	1.537
14TIFA2				
Diameter Deviations (*nm*)	0.05	0.10	0.15	0.20
Delay Variation (E-11)	0.740	1.394	2.124	2.693
Power Variation (E-6)	0.015	0.025	0.042	0.056
PDP Variation (E-16)	0.549	1.018	1.541	1.947

6. Conclusion

Full Adder cell plays an essential role in determining the performance of entire digital systems such as microprocessor, digital signal processor (DSP), microcontroller, and so forth. In fact, it is applied almost in all larger arithmetic circuits such as variant types of adders, subtractors, multipliers, etc. Therefore, by enhancing the hardware parameters of this cell we will improve the performance of portable consumer electronics such as laptops, tablets, notebooks, personal digital assistants (PDAs), cellular phones and so many forth.

Recently approximate computing has extensively attracted the attention of circuit designers and researchers to design energy-efficient circuits by relaxing exactness for some outputs. This method can be used in fault-tolerant applications such as multimedia, image processing, pattern recognition, machine vision or learning, and so forth where either human perception is limited to understand faulty outputs or faulty output is not critical.

In this paper, we proposed two novel efficient inexact 1-bit Full Adder cells using carbon nanotube field effect transistors (CNFETs). The proposed designs were called 14TIFA1 and 14TIFA2 which had only 14 transistors. Extensive computer simulations were conducted to evaluate the efficiency of circuits at both application and switching levels of abstraction. At the application level, Full Adders were applied in motion detector as one of the image processing applications, and peak signal to noise ratio (PSNR) was taken into account. Results confirmed that the proposed cells have close completion with their counterparts. Also, comprehensive simulations at switching level at different power supplies, output loads, and ambient temperatures were carried out. Again, simulation results confirmed the superiority of the proposed cells in terms of delay, power delay area product (PDAP), and power delay area PSNR product (PDAPP) metrics. Finally, the robustness of the proposed cells was studied in the presence of process variation using *Monte Carlo* transient analysis. Simulation results depicted the robustness of the proposed cells in the presence of diameter mismatches of carbon nanotubes (CNTs).

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Paper Handling Data:

Submitted: 10.12.2019
Received in revised form: 09.10.2021
Accepted: 09.19.2021
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