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Short Paper

An Efficient OHR Subtractor Circuit

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Abstract

Abstract-Residue Number System (RNS) is an appropriate system for arithmetic operations because of high speed execution during their calculation. If a one-hot residue number (OHR) system instead of pure residue is used, this speed is increased. There is a problem in OHR with large hardware modulo. Because of using barrel shifter structure in OHR, the subtract circuit has a hardware complexity in the order of m^2 in which m is the selected modulo. In this paper a new structure is introduced for subtract operation in OHR whose hardware is in the order of $m^2/2$, compare to original m^2.

Keywords: One Hot, Modular Subtract, Residue Number System, Arithmetic Operation.

1. Introduction

Our goals in VLSI circiut design is to decrease size and power consumption and to increase speed of a design. In order to reach these goals in arithmetic operations, a residue number system (RNS) is used. RNS has a great potential in Digital Signal Processing, Fast Fourier Transform (FFT), Ad-Hoc Networks and other applications.

There is another generation for RNS which named one-hot residue number(OHR) system. Using this system in arithmetic operations increases the speed and decreases the propagation delay of the design. A subtractor in OHR has a delay equal to one transisor and amount of hardware is in the order of m^2 in which m is the selected modulo [1-3].

In [4] we introduced a new design for OHR adder and in this paper a new design for OHR subtract circuit is presented in which amount of hardware is decreased to half .

The rest of paper is organized as follows. In section 2, a background on one-hot residue number system and its modular subtract circuit is introduced. In Section 3 the proposed efficient subtractor in an OHR system is presented. In section 4, comparision between conventional subtractor in the OHR and new design is shown.

2. Background

A RNS system is based on a set of module as $P= \{m_1, m_2, \dots m_L\}$. Each natural number is presented in residue number system with a set of number as $X=\{x_1, x_2, x_3, x_L\}$, where $x_i=X$ mod m_i, for $i =1, 2, L$. Range of numbers which can be presented in this system is $[0, M-1]$ where $M= m_1 m_2 m_3 \dots m_L$.

An arithmetic operation on two operands, $X=\{x_1, x_2, x_3, x_L\}$, $Y= \{y_1, y_2, y_3, y_L\}$ can be done in RNS using Eq. (1), in which 'o' denotes add, subtract or multiply operations.

$$Z= XoY \text{ and } Z=\{z_1, z_2, z_3, \dots, z_L\} \text{ then } z_i =\langle x_i \text{ o } y_i\rangle \quad (1)$$

The performance of RNS systems are improved using a one-hot system. This method is called the one-hot residue (OHR) number system. Circuits in an OHR system is fast, simple and independent to module. In a one-hot residue number system each number in modulo m_i is presented with m_i lines, which are numbered from 0 to m_i-1. Each number activates its corresponding line.

A subtractor circuit in an OHR system is implemented using a barrel shifter. It has two inputs which are called, *input1* and *input2*. These two inputs are in modulo *m*. The circuit subtract input1 from input 2. In Figure 1 structure of subtractor circuit in an OHR system for modulo *5 (m=5)* is shown .

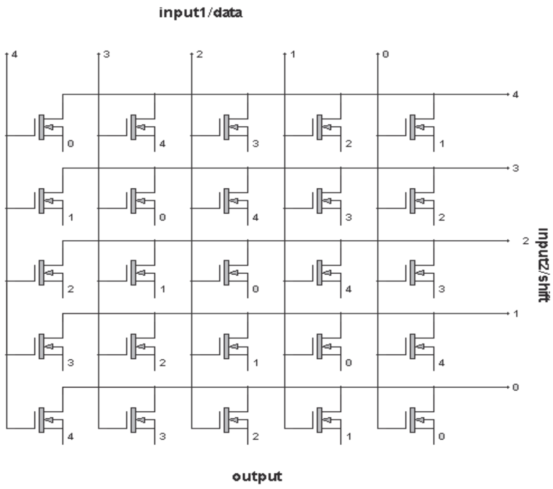

Figure 1. Structure of a subtractor circuit in OHR system for modulo 5

Propagation delay for this circuit is equal to propagation delay of one transistor. Total number of needed transistors is equal to m^2. In this design m^2 *is* equal to *25* [5-6].

In this paper a new design for OHR subtractor will be presented in which amount of needed hardware is about half of the conventional one.

3. The Proposed OHR Subtractor Circuit

Conventional design for the subtractor in an OHR system has the area problem when the selected modulo is big. For solving this problem in this section a new design is presented.

Consider that the selected modulo is *m*. *a* and *b* are two inputs for modular subtract circuit and *c=b-a* is its output, all less than m $(0 \le a, b, c < m_i)$.

Figure 2 shows the new design for a subtractor in OHR with selected modulo *5(m=5)*.In this method, a structure similar to barrel shifter is used. *a* and *b,* as inputs of circuit will cause two situation. In situation one, input 1 of the multiplexer is selected and one of the transistors on the diagonal is 'ON' and its output will appear on the output of multiplexor. In situation two, outputs of the entire parallel transistors in right side of Figure 2 are inactive; therefore input 0 of multiplexer is selected. In this situation one of the transistors below diagonal is 'ON'. According to selected input of multiplexer, output of this active transistor is appeared on the output pins of circuit.

For example, consider selected modulo is *5*, *a=00100(in OHR) =2(in decimal)* and *b=00100(in OHR) =2(in decimal) are the inputs*, and then Output of parallel transistors is *00100*. In this case, zero means high impedance. Therefore the input 1 of multiplexer is selected. On the barrel shifter just one of the transistors on the diagonal is 'ON' and its output is ‘1’. The result is appeared on the output of multiplexer, which is equal to *00001(in OHR) =0(in decimal).*

For another example consider *a=00100(in OHR) =2(in decimal)* and *b=01000(in OHR) =3(in decimal).* All outputs of parallel transistors are inactive. Input 0 of multiplexer is selected. Inputs *a* and *b,* set one of the transistors below the diagonal to 'ON' and its output is ‘1’. At last c= b-a=0010(in OHR) =1(in decimal) is appeared on the output of multiplexor.

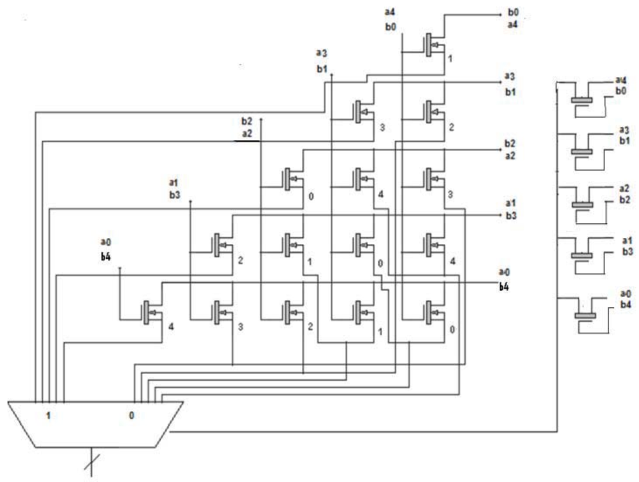

Figure 2. The proposed design for an subtractor in OHR for m=5

In Figure 3 simulation result of presented circuit in Figure 2 is shown. This simulation is done in HSPICE (w.2004.09). In this simulation selected modulo is m=5. First inputs are a=10000=, b=00100 in OHR which are equal to a=4 and b=3 in decimal. As a result of these inputs, v=b-a=10000 which is equal to v=3-4+5=4 in decimal is appeared on output pins. After that, inputs are changed to a=b=01000 in OHR which is equal to a=b=3 in decimal. Output is changed to v=00001 in OHR and 0 in decimal. Other signals which are not indicated in Figure 3 are all equal to zero.

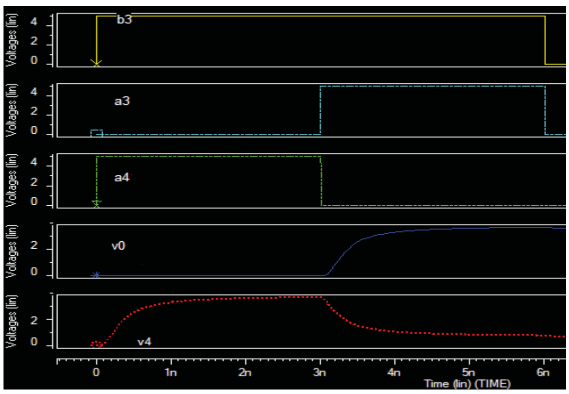

Figure 3. Simulation result of Figure 2.

In the next section, presented design in this section will be compared to the traditional design based on the propagation delay and amount of needed hardware.

4. Comparison

In this section conventional subtract circuit in OHR is compared with the new design proposed in this paper. Comparison is presented in two aspects, amount of needed hardware and the propagation delay.

If the selected modulo is m_i, then the number of needed transistors in conventional design for the subtractor is m_i^{r}. In the new design proposed in this paper this rate reduced to the order of $m_i^2/2+7m_i/2$, shown in Eq(2) .

$$(((m_i*m_i)-m_i)/2)+m_i+Tran_{mux}+m_i=m_i^2/2+7m_i/2 \quad (2)$$

A comparison between number of needed transistors in two designs shows that for $m_i>7$, the proposed method in this papers needs less hardware than traditional OHR subtractor circuit. Figure 4 shows the number of needed transistors in two designs versus the modulo values.

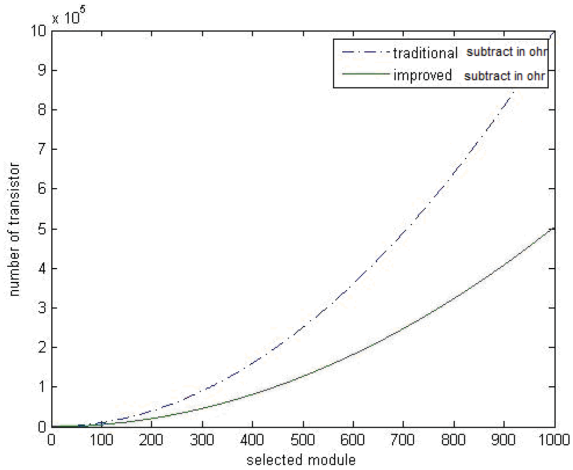

Figure 4. Comparison of needed hardware

The propagation delay in traditional design is equal to delay of one transistor and in proposed design is equal to delay of two transistors which both of them are small. In spite of increasing the propagation delay, decreasing the needed hardware is the main contribution of the proposed circuit.

5. Conclusion

In this paper, a new design for a subtractor in OHR system was proposed. The proposed circuit for the subtractor is decreased the amount of hardware to about half, compare to conventional OHR subtractor. The propagation delay in the new design is increased to two transistors.

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