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RF Resource Planning in Application Specific Integrated Circuits to Improve Timing Closure

Ali Mohammad Zarei[1] Ali Jahanian[2]

[1]Department of Electrical and Computer Engineering, Islamic Azad University-Qazvin Branch, Qazvin, Iran
[2]Department of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran

Abstract

VLSI technology scaling raised the new problems in conventional metal wires. Some new technologies and materials are proposed for modern interconnects such as optical interconnection, Nano-wires and radio frequency interconnection. In this paper, a new placement/planning approach is proposed for using the RF interconnects in regular ASICs. In the proposed approach, three placement configurations are examined for RF resources and electrical characteristics of the final circuit is compared. Our experimental results show that using a suitable RF planning, this technology can be suitable, especially for large and complex circuits. Approaches examine the best and suitable placement for RF interconnections making better slacks in paths and smaller total wire length in plan. In this work, three approaches for RF interconnection placements are proposed. Experimental results show that performance of attempted circuit can be improved by about 19% in cost of less than 5% area overhead.

Keywords: RF Interconnects, Placement, Performance.

1. Introduction

Scaling of the VLSI technologies improves the speed of active devices dramatically while global interconnects have become a limiting factor for performance and signal integrity of the complex circuits. Moreover, large number of long wires increases the routing congestion that may tend to problem in routing and signal integrity problems. Therefore, mitigating the troubles of the global interconnect is very critical for current and future VLSI design methodologies [1].

In recent years, some new interconnect technologies such as optical wires, Nano-wires and radio frequency interconnections are proposed to mitigate the drawbacks of electrical interconnects.

In optical interconnects, electrical signals are converted to optic signals at source (begin) of each wire and then, these signals are converted to digital data at the receiver after transmission via the on-chip optical fibers. The most important advantage of optical interconnections is the higher (carrier) frequency and the corresponding large photon energy. The higher carrier frequency (shorter wavelength, typically in 1µm range) allows us to use Optical fibers to send optical signals without high loss [2]. The main limitation of the optical fiber in current technology is that flexibility and routing ability of fiber optics are low and they are difficult to be fabricated [3].

Nanowires are a kind of wire that is scaled into Nano dimensions and come in two forms, Carbon Nano-tubes (CNTs), and Graphene Nano-ribbons (GNRs) [3, 4]. These materials have outstanding electrical properties including high motilities at room temperature, high current densities, and micron- scale mean free paths. There are many possible transistor designs involving CNTs and GNRs, and each offers a unique set of benefits. However, they face a number of challenges like difficult fabrication and very little parts face to ordinary elements [5].

Wireless/RF interconnects is another promising solution for the mentioned problems. Increasing operating frequency and die size have led to the concept of wireless/microwave communication which enables signal distribution through transmission lines at the speed of light (10ps/mm) with less dispersion across the band and less baseband interference [5-8]. On the other hand, using RF communications enables the routing reconfiguration on the chips [9]. In other words, variation of frequency bands and programmable specifications of RF transmitters and receivers have led to the routing configurability [9]. Moreover, using RF-interconnects improves testability (e.g. controllability and observation ability) of the circuits.

In related works we can explain that many researches are published about the physical specifications of radio frequency transceivers and limitation and challenges of them have been described.

In those researches there is a kind of information deficiency about physical placement algorithms and their challenges. However there are many basic and physical information and researches about RF interconnection but in placement method especially in RF planning this work is novel and previous researches are limited to some special usage (clock signal).

In this paper, we analyzed the possible plans for placement of RF routing resources in canonical ASIC design flow and propose an efficient planning for these resources. In this research, various plans for RF transceivers are analyzed in terms of the basic parameters and the most suitable plans are addressed. Our experiments show that total wire length and performance of the designs can be improved considerably using the presented RF plan. Finally we propose a placement based on resulted designs.

This paper is organized as follows. Section 2, have a survey on RF characteristics and its challenges. Section 3 is dedicated to our RF planning contribution. Section 4 is experimental results and illustrates our placement algorithms based on our planning designs. Finally the Section 5 concludes the paper.

2. RF Interconnection

The main idea of RF/wireless interconnects is transmitting data in the form of electromagnetic waves using integrated on-chip antennas. In such a system, a wave at radio or millimeter wave frequency propagates either through free space or guided mediums at the speed of light. Signal transmission through free space requires large-size antennas, so this method is not applicable for current designs. On the other hand, transmitting microwaves in guided mediums such as micro-strip transmission line (MTL) or coplanar waveguide (CPW) is more feasible due to its smaller antenna size and lower attenuation [10].

The RF concept is illustrated in figure 1 where mixers are used to modulate the carrier with digital data [11].

Since the area overhead of on-chip antennas reduces with increasing operating frequency; they can effectively replace the wired global interconnects in future ULSI designs running in the multi-GHz range [5]. In recent decades, printed antennas including micro-strip, dipole and loop antennas, fabricated on substrates; have drawn most attentions. There are several different types of on-chip antennas such as linear, folded, zigzag and meander, which among those, linear dipole and folded dipole structures are suitable as on-chip integrated antennas due to their compact size [10]. However, a higher power gain and a more compact implementation can be provided by combining different structures such as folded and meander.

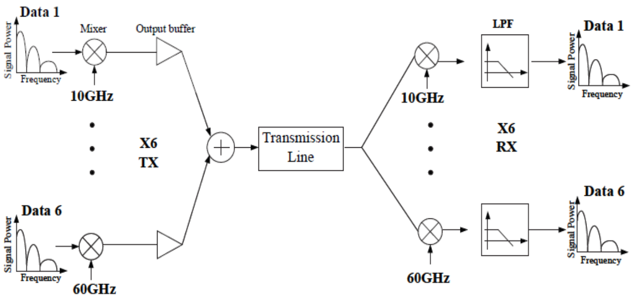

Figure 1. RF-I architecture [8]

In order to take the wave propagation characteristics under control, there are some common transmission line structures such as MTL or CPW. In CPW, there are two lines on each side of the signal line, used to implement the ground planes while in MTL, the signal line is in a top metal layer and the ground plane is either the silicon substrate or a low metal layer. Hence, in CPW, the ground planes can effectively shield the transmission lines against the exterior environment effects and also reduce the characteristic impedance by shortening the signal-ground distance. In this paper, CPW is supposed to be the transmission media.

The transmission line can be shared between multiple users at the same time by using frequency division multiple access (FDMA), code division multiple access (CDMA), or the combination of the two FDMA/CDMA. In FDMA, frequency spectrum is divided into different bands by using different carriers while in CDMA data streams is spread in the same bandwidth by using orthogonal codes[11]. Moreover, to improve data rate, a combined FDMA/CDMA (also referred to as multicarrier CDMA) is a possibility [12].

However, it should be noted that only a limited number of RF resources can be used due to their area and power consumption overhead. The aperture size of the antenna for efficient transmission in free space will be in the order of 1mm^{2}even at near 100GHz operating and cut-off frequencies. Although, this value in transmission through guided mediums is smaller considerably but it is still large enough to restrain the use of RF-interconnects. Therefore, some strategies should be made to distribute transceivers/receivers inside the integrated circuit such that they can be used efficiently. Moreover, feasibility of managing the interferences between the wires (or external sources) and RF-interconnects is approved in [10] by considering some design considerations such as CDMA and CFDMA coding.

3. RF-Resources Placement

An important factor in efficiency of RF-interconnects is the location of RF resources. They should be located at suitable places such that the terminals of critical and long wires are placed close to the transceivers. In this situation, critical and long wires may be routed using RF resources to reduce wires' delay and mitigate routing congestion. Three different approaches can be used for locating the RF resources:

- **Before Placement:** in this choice, RF resources are planned before placement in which suitable locations of

RF transceivers may be determined based on the statistical or empirical information. After the RF planning and before the cell placement, location of RF cells is fixed and other cells are placed. In this approach, standard cells can be placed regarding the RF location of transceivers such that long wires are routed using RF interconnects. Obviously, planned location of the RF transceivers is very important in this scenario.

- **After placement:** In this case, RF transceivers are inserted into design after placement of standard cells. This choice is not so feasible because RF resources are very large blocks and insertion of them after placement is efficient or even may not be feasible.
- **During placement:** In this scenario, RF resources are considered as regular standard cells and they are located during the cell placement concurrent with other cells of the design. The main drawback of this method is that current placement algorithms are not efficient when some of standard cells are very large size.

Our analyses and experiments show that after placement is not efficient because, RF cells are very larger than regular standard cells and inserting them into the circuit and place them between the placed cells updates bulk of the design and corrupts the optimization level of the design. We evaluated the RF planning (before placement) and RF/cell placement (during placement) in this research.

As mentioned before, this paper is dedicated to the last approach wherein RF resources are planned before the cell placement. The planed pattern of RF resources is crucial. Therefore, we analyzed various patterns for RF resource distribution in this section and rest of this section described our analysis based on possible plans for placement of RF routing resources in canonical ASIC design flow.

3.1. RF Resource Planning Before the Cell Placement

We placed a dozen of standard benchmarks with various RF resource distributions and analyzed the suitability and efficiency of the plans. Considerable contributions are reported of analyzing the distribution of various wire shapes. We analyzed the distribution of wire segments in the standard benchmarks. Table 1 shows the distributions of L-shape wire segments in IWLS benchmarks. In this table, columns *#Cells*, *#Nets* and *#Pins* represent the specifications of the benchmarks. These columns describe number of the cells, nets and pins of each benchmark. Column *NLS* represents the percentage of the nets that at least have one L-shape wire segment and column *LLS%* represents the percentage of the wire length of the nets contains at least one L-shape wire segment.

The statistical analysis depicted in table 1 is performed after placement of the attempted benchmarks. We used DragonPlacer as the cell placer in this research. It is worth noting that DragonPlacer uses hierarchical min-cut placement algorithm that is widely used in research and industrial applications [13].

As shown in table 1, considerable portion of wires in attempted benchmarks have L-shape wire segments. Therefore, we focused to the RF interconnects plans which cover the L-shape nets. In the first plan that called X-region, RF resources are distributed on a two diagonal regions as shown in figure 2. In this figure, supposed that RF resources are distributed on gray regions that make a shape similar to X. By this architecture, RF interconnects can connect many of the L-shape wires.

Table 1. Statistical information about wire shape distribution

BM	#Cell	#Net	#Pin	NLS%	LLS%
spi	3227	3276	94	84.14	95.65
des_area	4881	5123	306	82.02	94.41
tv80	7161	7180	48	78.93	94.03
mem_ctrl	11440	11560	269	86.58	96.82
ac97_ctrl	11855	11947	134	83.61	94.23
usb_funct	12808	12955	251	84.2895	95.25
b20	19107	19143	58	83.67	96.14
dma	19118	19807	950	86.45	96.34
wb_conmax	29034	30166	2548	81.44	94.44
ethernet	46771	46888	213	82.7	95.55
Average				**83.38%**	**92.29%**

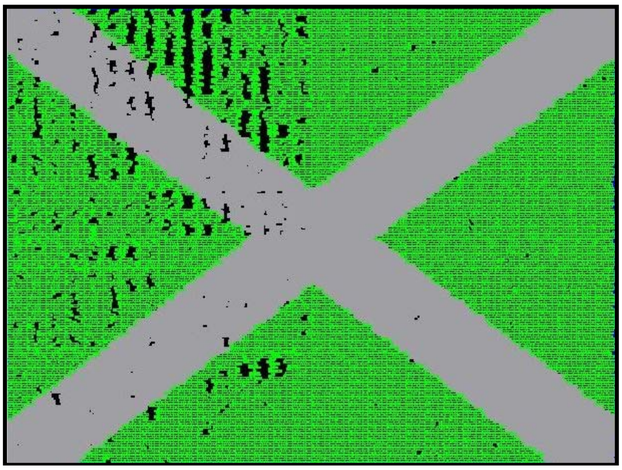

Figure 2. X-region RF planning

It seems that X-region RF planning, is suitable for those wires that go through the center of the design and it can distributes the RF resources through a two diagonal region. Our X-region is based on two diagonal strips which strips are in proportion by design width and it is in the centre of the design. Next section, experimental results, show that this plan is not very efficient because may of wires are laid on the out of the X-regions.

The second plan is called diamond-shaped as shown in figure 3. Diamond-shaped plan can be useful for crisscross wires because it can cover all the wires brink side and out of the design centre. Diamond shape is based on some concentric diamonds. In our work we use three concentric diamonds which width of each strip is in proportion of design width.

Each pinnacle of the diamonds is in the middle of the design. Our work uses three diamonds because of widespread form of this shape.

The third analyzed planning architecture is called as Grid-based RF planning. It covers all the chip area uniformly as shown in figure 4. This plan is made by nine vertical and horizontal strips and each area is equal the other ones. As it be seen and described in next section, this architecture is more efficient rather than two others (Figure 4).

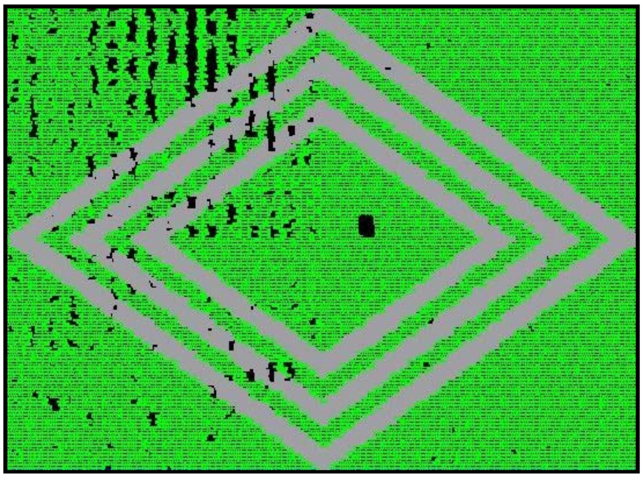

Figure 3. Diamond-region RF planning

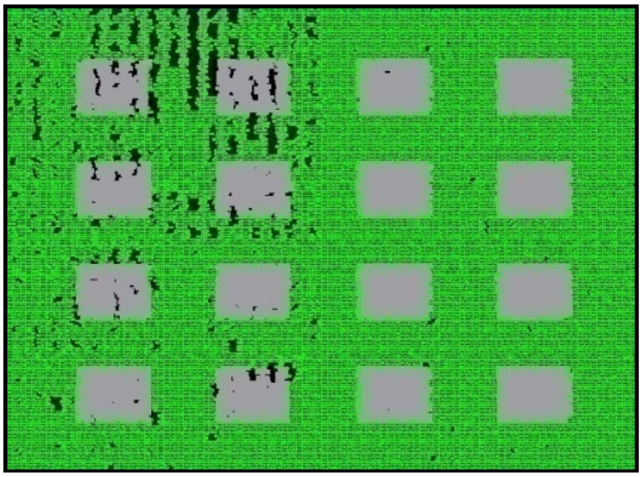

Figure 4. Grid-based RF planning

3.2. RF Resource Planning During the Cell Placement

Our analyses and experiments show that pre-placement RF planning is not efficient and concurrent RF/Cell placement may be more effective. We proposed a simulated annealing-based placement algorithm to determine the location of RF resource as well as standard cells. figure 5 shows the proposed during-placement RF planning algorithm.

As shown in figure 5, gray part is added to the canonical simulated annealing-based placement id revised to place the cells aware of RF resources locations. Gray section this figure, represents the revised section. RF resources are planned by X-region, Diamond-shaped and Grid-based before the cell placement algorithm. After each perturb, location of moved cells are checked.

If new location is far from RF resources, perturb is canceled. By this simple heuristic, cells are pushed to near the RF resources. Therefore, more number of terminals are place near the RF transceivers and using the RF interconnects will be more efficient.

Proposed during-placement RF resource planning

```
Step 1:          Initial_placemet();
Step 2:          $t=t_{init}$;
Step 3:          WHILE ($t > t_{final}$)
Step 3-1:            WHILE (inner_loop_cond = TRUE)
Step 3-1-1               $C_1$= Cost();
Step 3-1-2:              Perturb(cellx);
Step 3-1-3:              $C_2$=Cost();
Step 3-1-4:              $\Delta C = C_2 - C_1$;
Step 3-1-5:              IF  ($\Delta C >= 0$)
Step 3-1-6:              r = random(0,1);
Step 3-1-7:              IF (r < exp(-DeltaCost/t))
Step 3-1-7-1:                RejectPerturb(cellx);
Step 3-1-8:              END IF
Step 3-1-9:              IF(cellx is near to wireless resource)
Step 3-1-9-1:                IF(the net  cellx is in (netz) , doesn't
                             another cell near to wireless resource)
Step 3-1-9-1-1:                  RejectPerturb(cellx);
Step 3-1-9-1-2:                  RFnetlist<= netz;
Step 3-1-9-2:                END IF
Step 3-1-10:             END IF
Step 3-2:            END WHILE
Step 3-3:            $T = t * \alpha$;
Step 4:          END WHILE
```

Figure 5. Proposed during-placement RF resource planning

4. Experimental Results

As mentioned before, we have analyzed various plans for RF resources placement to explore an efficient configuration for the RF resources. We implemented our analysis algorithm with Edu CAD physical design system [14, 15], a Linux-based educational physical design platform, on an Intel 2.4 GHZ Core 2 Duo CPU with 2GB RAM. Ten circuits from IWLS benchmark suite are selected to evaluate the proposed method. Three first columns of the table 1 represent the specifications of attempted benchmarks.

Before analyzing the various RF configurations, the distribution of number of terminals is analyzed. Table 2 shows the distribution of the nets in terms of the number of their terminals. Columns *2TN* to *7TN* represent the percentage of the nets consist of 2 terminals to 7 terminals and the last column shows the nets with more than 7 terminals.

Table 2. Statistical analysis on terminal number distribution of wires

BM	2TN	3TN	4TN	5TN	6TN	7TN	More
spi	38.3	11.4	4.1	3.1	1.9	2.2	39.1
des_area	63.2	15.5	5.6	4.5	2.4	1.5	7.3
tv80	64.8	14.9	6.2	3.7	3.2	1	6.2
mem_ctrl	71.8	11.5	3.5	2.6	1.4	1.5	7.7
ac97_ctrl	72.1	7.5	11.6	2.4	1.1	0.4	4.9
us0b_funct	68.2	13.6	8.9	4	1.5	0.7	3.2
b20	62.2	15.7	9.4	4.7	3	1.5	2.5
dma	68	7	9	4	1	0.7	10.4
wb_conmax	67.8	8.8	4.4	3.1	1.3	1.1	13.5
ethernet	69.4	2.9	20.4	2.3	0.5	0.3	4.3
Average	**64.60**	**11**	**8.30**	**3.50**	**1.70**	**1.10**	**10**

As can be seen in table 2, major portion of the nets in the benchmarks have lower than 5 terminals (e.g. 90% of the nets have lower than 5 terminals). Therefore we analyzed the 2-, 3-, 4-, and 5-terminal nets in our analyses.

As can be seen in table 1, most of the wire segments are in L shape. So we can realize orthogonal plans can cross these segments. But most of the wires are in two terminal forms so a diametrical plan can cover these segments. After all, none-orthogonal plans can be in different form. So we can explain many plans.

We used the slack information in every routed wire to measure the delay improvements. After placement and routing in a benchmark design files each segment wire in the design take a slack number. Therefore, the critical paths are the segment with zero slack ones and segments with near the zero slack are the near critical path. So wire segments with zero slack or near zero slacks are the main target for our work (*Delay calculation= Previous Delay – Near critical path delay*). Table 3 shows the slack information in each benchmark in special plan called Grid-based. Each column is the number of nets with special ranges of slack.

Table 3. Slack information of wire segments in grid-based planning

BM	**S= 0**	**0<S≤5**	**5<S≤20**	**20<S≤50**	**50<S≤100**	**100<S≤300**	**300<S≤1000**
Spi	3	1	1	1	2	30	62
des_area	2	0	0	0	2	14	82
tv80	3	0	1	0	0	14	28
mem_ctrl	7	0	0	1	0	12	80
ac97_ctrl	9	0	0	0	3	27	42
usb_funct	18	0	2	4	0	0	37
b20	5	0	0	1	5	8	35
Dma	17	0	0	0	9	14	36
wb_conmax	3	0	0	0	2	5	89
Ethernet	1	0	0	0	0	7	25

As it can be seen in table 3 the most number of the wire segments are in range of the >300 and ≤1000. Statistical information of tables 1 to 3 is used for RF resources planning in this contribution. The following sub-sections describe the results of the analyzed RF configurations in terms of total wire length and critical delay.

4.1. RF Planning Before Placement

In this strategy, RF resources are placed before the cell placement and in this subsection; the X-region, Diamond-shape and Grid-based RF plans are evaluated in terms of total wirelength, delay and area.

4.1.1. X-Region RF Planning

As mentioned before, each X-region is made by two stripes that their width is about 0.6 of the design width and it is in the centre of the design. In our experiments, X-region area is about 20% of whole area. Table 4 shows the estimated total wire length improvement. RF transceivers are planned in the X-region configuration with attempted benchmarks. In table 4, column *RFN* shows the number of nets that are laid inside the X-region. We supposed that these nets can use RF resources. Columns *TWLB* and *TWLA* represent total wire length before and after RF routing and finally, column *TWLI* shows the total wire length improvement using RF interconnects.

Table 4. Experimental results of x-region RF planning in terms of total wirelength

BM	**RFN**	**TWLB**	**TWLA**	**TWI (%)**
spi	100	245642	208688	15.04
des_area	100	396997	357319	9.99
tv80	44	670745	616161	8.14
mem_ctrl	100	1093268	1000856	8.45
ac97_ctrl	100	1136943	1120404	1.45
usb_funct	96	1311037	1288836	1.69
b20	34	2087258	2006389	3.87
dma	72	2528568	2448637	3.16
wb_conmax	100	2851998	2748753	3.62
ethernet	100	699395	649824	7.09
Average	**84.6**			**6.25%**

As can be seen in table 4, total wire length improvement of X-region RF planning is not considerable.

Table 5 shows the estimated delay of improvement in the X-region RF planning. In this table, columns *CDB* and *CDA* represent total wire length before and after RF routing and finally, column *CDI* shows the total wire length improvement using RF interconnects.

Table 5. Experimental results of x-region architecture in terms of critical delay

BM	**#RFN**	**CDB**	**CDA**	**CDI(%)**
spi	100	3570.9	2920.91	18.2
des_area	100	4354	3704.03	14.92
tv80	44	6211	4710.96	24.15
mem_ctrl	100	4634.9	3984.88	14.02
ac97_ctrl	100	3141.9	2491.87	20.68
usb_funct	96	4315.5	3665.52	15.06
b20	34	7795.8	6295.75	19.24
dma	72	6106.6	4606.55	24.56
wb_conmax	100	4457.3	3807.33	14.58
ethernet	100	6122.8	5472.82	10.61
Average	**84.6**			**17.60%**

As can be seen in table 5, delay improvement in this case is better than total wire length improvement because many of critical paths are laid on X-region.

4.1.2. Diamond-Shaped RF Planning

Diamond-shape plan has three concentric diamond areas. Width of each strip consisting in each Diamonds is about 0.3 of width of design. The pinnacle of the diamond is in the middle of the design. With these calculations the Diamond-based area is about 20% of whole area. In table 6 we determine the improvement of the ten designs when we insert RF transceiver in Diamond-shaped mode.

In table 6, RFN is number of the nets exchanged by RF transceivers and Columns *TWLB* and *TWLA* represent total wire length before and after RF routing and finally, column *TWLI* shows the total wire length improvement using RF interconnects.

As can be seen in table 6 the TWI is not considerable. Table 7 shows the estimated delay of improvement in the Diamond-shaped RF planning. In this table, columns *CDB* and *CDA* represent total wire length before and after RF routing and finally, column *CDI* shows the total wire length improvement using RF interconnects.

Table 6. Diamond-region experimental results in terms of total wire length

BM	RFN	TWLB	TWLA	TWI (%)
spi	100	245642	2901435	3.18
des_area	100	396997	357997	9.82
tv80	49	670745	625718	6.71
mem_ctrl	100	1093268	1001543	8.39
ac97_ctrl	87	1136943	1120953	1.4
usb_funct	95	1311037	1287535	1.79
b20	50	2087258	2025518	2.957
dma	73	2528568	2453624	2.963
wb_conmax	100	2851998	2750933	3.54
ethernet	28	699395	6913404	3.73
Average	**78.2**			**4.45%**

Table 7. Diamond-region experimental results in terms of critical delay

BM	#RFN	CDB	CDA	CDI(%)
spi	100	3570.9	2920.91	18.2
des_area	100	4354	3704.03	14.92
tv80	49	6211	4710.96	24.15
mem_ctrl	100	4634.9	3984.88	14.02
ac97_ctrl	87	3141.9	2491.87	20.68
usb_funct	95	4315.5	3665.52	15.06
b20	50	7795.8	6295.75	19.24
dma	73	6106.6	4606.55	24.56
wb_conmax	100	4457.3	3807.33	14.58
ethernet	28	6122.8	4622.8	24.5
Average	**78.2**			**18.99%**

4.1.3. Grid-Based RF Planning

Grid-based plan is made by nine vertical and horizontal slice of design. So each Grid is equal to others. With these calculations the Grid-based area is about 20% of whole area. But first we have a analyzing on number of nets in some designs. Most of the wires are two-terminal wire (As it is shown in table 2). For this reason we focused on two terminals of the wire.

When two terminals of the wire are in the Grid-based plan (or other plans), it is nominated for replacement with RF transceivers. Wires with more than two terminals in plan are nominated with proportion calculations.

In table 8 we determine the improvement of some designs when we insert RF transceiver in Grid based mode. In this table RFN is the number of the nets that are exchanged by RF transceiver. Columns *TWLB* and *TWLA* represent total wire length before and after RF placement and finally column *TWI* shows the total wire length improvement.

As you see the average TWI is about 5% and is negligible but it is a supplement improvement versus delay improvement in next table. In table 9, columns *CDB* and *CDA* critical delay before and after RF routing and finally, column *CDI* shows the total wire length improvement using RF interconnects.

Finally for placement algorithm, we focused on Grid-based design, because of wide spread strategy and its reconfigurable form.

Table 8. Grid-based experimental results in terms of total wire length

BM	RFN	TWLB	TWLA	TWI (%)
spi	100	245642	213523	13.07
des_area	100	396997	360236	9.25
tv80	46	670745	626171	6.64
mem_ctrl	100	1093268	1004446	8.12
ac97_ctrl	81	1136943	1119383	1.54
usb_funct	61	1311037	1289305	1.65
b20	54	2087258	2031032	2.69
dma	76	2528568	2455771	2.87
wb_conmax	94	2851998	2755178	3.39
ethernet	33	699395	6908003	3.81
Average	**74.5**			**5.30%**

Table 9. Grid-based experimental results in terms of critical delay

BM	#RFN	CDB	CDA	CDI(%)
spi	100	3570.9	2920.91	18.2
des_area	100	4354	3704.03	14.92
tv80	46	6211	4710.96	24.15
mem_ctrl	100	4634.9	3984.88	14.024
ac97_ctrl	81	3141.9	2491.87	20.68
usb_funct	61	4315.5	3665.52	15.06
b20	54	7795.8	6295.75	19.24
dma	76	6106.6	4606.55	24.56
wb_conmax	94	4457.3	3807.33	14.58
ethernet	33	6122.8	4622.8	24.5
Average	**74.5**			**19.01%**

4.2. RF Planning During Placement

As mentioned before, we proposed an RF-aware placement algorithm in which RF resources are placed as well as the regular standard cells. Our final results for X-region, diamond-shaped and Grid-based are shown in table 10, table 11, and table 12. In each table, first column is wire length improvement (about 6.22% for Grid-based) and second one is delay improvement (about 11.21% in-Grid based).

Table 10. X-region RF placement results in during placement strategy

BM	Wirelength improvement (%)	Delay improvement (%)	Area overhead (%)
spi	-	-	35 (small)
des_area	-	-	32 (small)
tv80	-	-	16.5 (small)
mem_ctrl	5.49	5.53	11.01
ac97_ctrl	6.01	6.23	7.38
usb_funct	6.11	5.51	7.39
b20	5.99	4.75	6.73
dma	5.85	9.6	6.59
wb_conmax	6.99	4.58	6.25
ethernet	8.75	8.93	2.27
Average	**7.31%**	**6.43%**	**6.80%**

Table 10 is about X-region placement algorithm and results 7.31% and 6.43% and 6.80% in total wire length, delay and overhead concepts.

Table 11. Diamond-shaped RF planning results in during placement strategy

BM	Wire length improvement (%)	Delay improvement (%)	Area Overhead (%)
spi	-	-	36.21 (small)
des_area	-	-	31.12 (small)
tv80	-	-	20.31 (small)
mem_ctrl	2.49	6.59	09.65
ac97_ctrl	4.43	8.42	09.33
usb_funct	3.99	7.53	8.38
b20	4.71	6.52	10.59
dma	5.85	10.43	7.5
wb_conmax	4.98	5.95	5.99
ethernet	6.56	10.38	1.99
Average	**4.71%**	**7.97%**	**7.63%**

Table 11 shows the results of diamond-shaped placement algorithm and results 4.71% and 7.97% improvement in total wire length and delay corresponding with7.63% in area overhead.

Table 12. X-region RF planning results in during placement strategy

BM	Wire length improvement (%)	Delay improvement (%)	Area Overhead (%)
spi	-	-	40.47 (small)
des_area	-	-	36 (small)
tv80	-	-	24.58 (small)
mem_ctrl	4.13	8.31	14.77
ac97_ctrl	5.51	11.13	11.73
usb_funct	5.54	10.14	12.52
b20	5.62	10.36	12.33
dma	7.5	13.12	8.52
wb_conmax	6.43	9.06	7.87
ethernet	8.81	16.41	2.60
Average	**6.22%**	**11.21%**	**10.04%**

Table 12 is about diamond-shaped placement algorithm and results 6.22%, 11.21% and 10.04% in total wire length, delay and overhead concepts. At the end we have area overhead and it is just about 10.4%. For RF transceiver with a large area usually it can be a acceptable overhead. In table 12 (and table 10 and table 11), there are blank results in benchmark files with little size. In these cases we can’t use our placement because of small size of the inputs. It’s usually caused by small size and limited numbers of the cells in a design file to exchange the cells and cost comparison in SA algorithm with huge RF transceivers. So we understand this approach is suitable for big inputs with huge number of cells.

5. Conclusion

After size shrinking in circuits, there are some huge problems with its backwashes. So the need of a new way to make connection between two terminals in circuits such as optical interconnection and RF interconnection has been sensed. In this work we focused on RF interconnections and a new approach for RF interconnection placement.

Our paper is about RF interconnection planning that means the placement of RF trans-receivers is based on analyzing the many our placed design with a specific placement algorithm. It shows the experimental results of three proposed plans, and suggests this approach for RF trans-receiver placement because this work is based on analyzing the same design in same placement algorithm with number of repetitions. Finally we proposed new placement algorithm for RF interconnection based on proposed plans. Final placement with 10 number practical benchmark files results about 11.21% and 6.22% improvement in delay and wire length (in Grid-based). This work is novel placement approach for a novel interconnection in physical design. Future works can be a new placement with different algorithm but this work shows that a widespread planning strategy like Grid-based, can be used in RF transceiver placement.

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Ali Mohammad Zarei received the B.Sc degree in Computer Engineering from University of Sadjad of Mashhad, IR-Iran in 2010 and the M.Sc degree in Computer Engineering at Islamic Azad university of Qazvin, IR-Iran in 2012. His current research interests are focused on VLSI design automation, FPGA Architecture, and Embedded Systems Design.

E-mail: amzarei@qiau.ac.ir

Ali Jahanian received the B.Sc. degree in Computer Engineering from University of Tehran, Tehran, Iran in 1996 and the M.Sc. and Ph.D. degrees in Computer Engineering at Amirkabir University of Technology, Tehran, Iran in 1998 and 2008, respectively. He joined Shahid Beheshti University, Tehran, Iran in 2008. His current research interests are focused on VLSI design automation, Biochips and Automotive embedded system design.

E-mail: jahanian@sbu.ac.ir

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Corresponding author: Ali Mohammad Zarei,
Islamic Department of Electrical and Computer Engineering, Islamic Azad University-Qazvin Branch, Qazvin, Iran.