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Novel ternary multipliers improved in size and performance based on carbon nanotube transistor

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Abstract

The multiplier is the basic computational operation in ALUs and impacts on their performance and chip size. Carbon nanotube field effect transistors (CNFETs) are used in many designs to enhance their performance, area, and power dissipation. Moreover, using CNFET results multi-value logic (MVL) -i.e., ternary logic. Using ternary logic in circuits results in chip size reduction due to its less connection than binary logic. In this paper, two novel ternary multipliers based on CNFET are proposed. The number of transistors is reduced about 15% in the first proposed design compared with the best-reported result. The PDP of the second proposed circuit is reduced about 57% in comparison with the best design. Stanford's 32-nanometer model, the HSPICE software, and same input signals are used to investigate the criteria of simulation of multiplier circuits.

Keywords: Multiplier, CNFET, MVL, Ternary

1. Introduction

Today, mobile electronic devices are used in many aspects of work. Besides the need for smaller electronic parts, power and performance are two critical criteria in these devices. Building the processors with CMOS technology has encountered limitations such as power consumption, parametric variations and gate control [1]. Therefore, to meet the new needs, it is necessary to use other technologies. One of the new technologies that could be used instead of CMOS is carbon nanotube field effect transistor (CNFET) technology presented by Ijima in 1991 [2]. This technology may be helpful in the reduction of the processor's dimensions, transistor delays, and power consumption, and also it can be used to design three-value circuits [3], [4]. Changing the diameter of the nanotubes lead to creating transistors with the desired threshold voltage, therefore we can have system design with multi-value logic [3], [4].

The more technology size gets smaller, the more circuit connectivity becomes the important factor in chip area [7]. Computational performance would be increased by using multi-value logic instead of binary logic, while it's possible to send more information through fewer wires [5], [6].

Multipliers should affect the speed of many computational circuits [8]. Multiplier circuits are the slowest part of many computational systems, and also it occupies a large area on chips [5]. Therefore, criteria such as area and latency are considered when a multiplier is designing.

In this paper, two multipliers are introduced. The first proposed design has a smaller number of transistors and the second one has less PDP.

A brief description of the CNFET is in Section 2. Ternary logic is introduced in Section 3. The proposed designs are described in Section 4. Comparisons and results are presented in Section 5. Finally, the paper is concluded in section 6.

2. Carbon nanotube field-effect transistor

The CNT (Carbon Nano Tube) is called a graphite plate, which has a thickness of one carbon atom in the form of a cylinder [9]. Graphite plates are made of a hexagonal network

of carbons. Carbons are the fourth most abundant element in the world and have atomic number 6 [10].
There are two kinds of carbon nanotubes, one of them is a single-wall nanotube (SWNT) and another is a multi-wall nanotube (MWNT) [11]. A carbon nanotube field effect transistor (CNFET) is a transistor whose communication channel is through carbon nanotubes.
CNFETs have some advantages over silicon transistors, such as faster speeds, more scalability, lower power consumption and also same electrons and holes mobility which simplifies transistor sizing [12]. Another advantage of CNFETs is an adjustable threshold which should be done by changing the diameter of the nanotubes. Multi-value logic circuits could be designed by this property of CNFET [11].
Characteristics of carbon nanotubes are influenced by the chiral vector, which is indicated by the (n, m) indices. If the difference between the chiral vector indices is a multiple of three, the nanotubes are metal and otherwise, it acts as a semiconductor [13].
The diameter of the nanotube should be adjusted by specifying the chiral vector parameters. The formula that is used to calculate the nanotube diameter is given in Equation (1) [14]:

$$D_{CNT} = \frac{\sqrt{3}\alpha}{\pi}\sqrt{m^2 + m \cdot n + n^2} \qquad (1)$$

In the above equation 'α' is a distance between two adjacent carbon atoms, which is equal to 0.14 nm.
The threshold voltage of CNFETs is depended on CNT diameter and it is computed through the following formula [14]:

$$V_{th} = \frac{\sqrt{3}\alpha V_{\pi}}{3e\, D_{CNT}} \approx \frac{\alpha}{D_{CNT}} 3.0333 \qquad (2)$$

In the equation 2 'e' is electron charge and Vπ (~3.033 eV) is the carbon π-π bond energy in the tight bonding model CNFETs width would be calculated by equation (3) [14]:

$$w \approx Min\,(Wmin, N \times Pitch) \qquad (3)$$

W_{min} is the minimum width that be applied according to lithography limitation. N is the Number of nanotubes in the channel. Pitch is the distance of centers of two adjacent nanotubes in the channel. Fig. 1 shows the schematic of a carbon nanotube field-effect transistor.

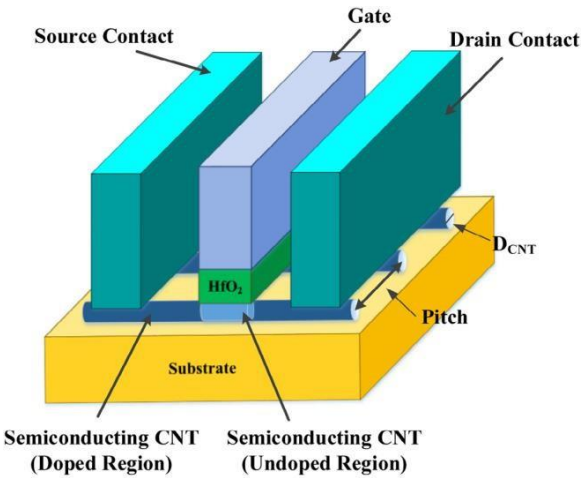

Fig. 1. Schematic of a carbon nanotube field-effect transistor [2].

There are three types of carbon nanotube transistors. One kind of them is Schottky Barrier (SB) transistors. In this type, conduction is performed by direct tunneling on the source and channel connection [15], [16]. The second type is MOSFET-like CNFET which is unipolar and its behavior is like MOSFET with higher performance. Unlike SB-CNFETs, this type of transistor has not Schottky Barrier in ON mode.
The third type is band-to-band tunneling CNFETs. These kinds of the transistor are suitable for low-power circuits due to their cut-off characteristics and low current in ON mode [17].
Due to the similarity between MOSFET-like CNFET and MOSFET, the two proposed multiplier circuits in this paper is designed with these transistors instead of MOSFETs.

3. Review of ternary logic

If multi-level signals are used in a digital circuit, then it is called a multi-value logic circuit. Using multi-value logic has advantages over binary logic. In the binary logic integrated circuits about 70% of the chip area is allocated to internal connections, about 20% of the area is used for insulation and only 10% is used for active circuits [7]. The amount of data to be sent on a wire simultaneously would be increased if multi-value logic is used. Therefore, using multi-value logic may reduce the number of wires and their connections required for data transmission.
Radix e=2.718 is the best radix for effective implementation, but due to the hardware constraints, integer radix should be used. The closest integer, i.e., radix 3, are selected and called ternary logic [18], [19].

Voltage level	Logic value
0	0
$\mathbf{1/2}\ V_{dd}$	1
V_{dd}	2

Table 1. Logic symbols [20]

Ternary logic (three-value logic) is a kind of multi-value logic and has the advantages of the multi-value logic. The symbols that are used in this logic and their related voltage are given in Table 1. The basic operation of this logic is inverting. Three types of inverting operation should be used; the standard

ternary inverters (STI), negative ternary inverters (NTI), and positive ternary inverters (PTI). The truth table of the inverters is shown in Table 2.

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 2. True table of STI, PTI and NTI [20]

4. The proposed multipliers

In this section, two novel ternary multiplier circuits are proposed. These circuits are designed with CNFETs with adjustable threshold voltage characteristic. The truth table of the multiplication operation in radix three is shown in Table 3.

A	B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

Table 3. Ternary multiplier true table

Both proposed multiplier circuits consist of main body and preamble circuits. The outputs of the preamble circuits are given to the main body and the main body generates the final output results.

Several logic circuits are introduced at the transistor level, where their outputs should be used in the main body of the multipliers. A negative ternary NAND (NT- NAND) is designed based on the negative ternary invertor in [20]; this circuit will have zero output if none of its inputs are zero.

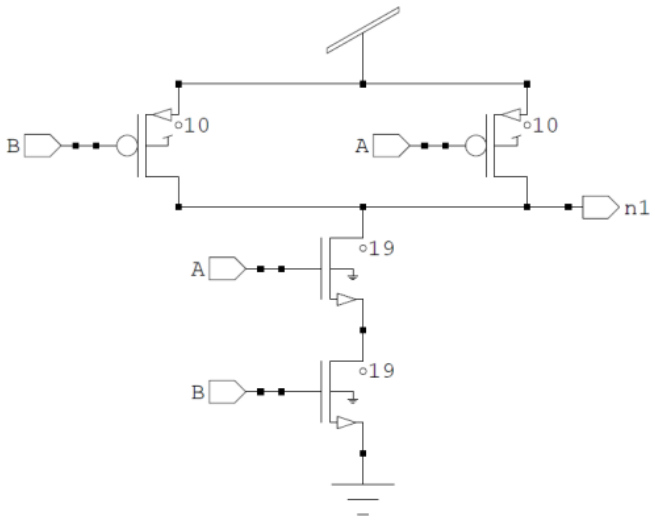

Fig. 2. Negative ternary NAND (NT-NAND)

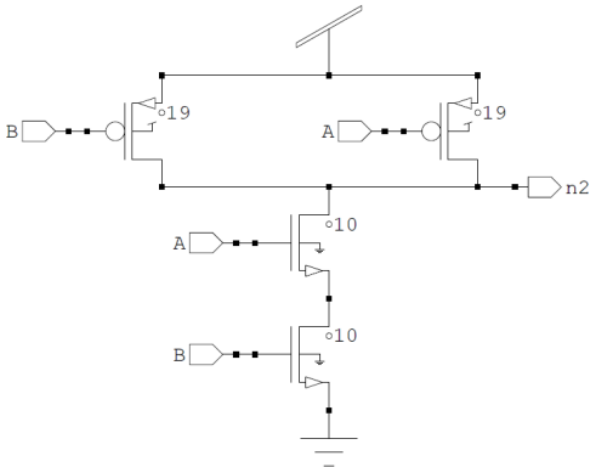

Fig. 3. Positive ternary NAND (PT-NAND)

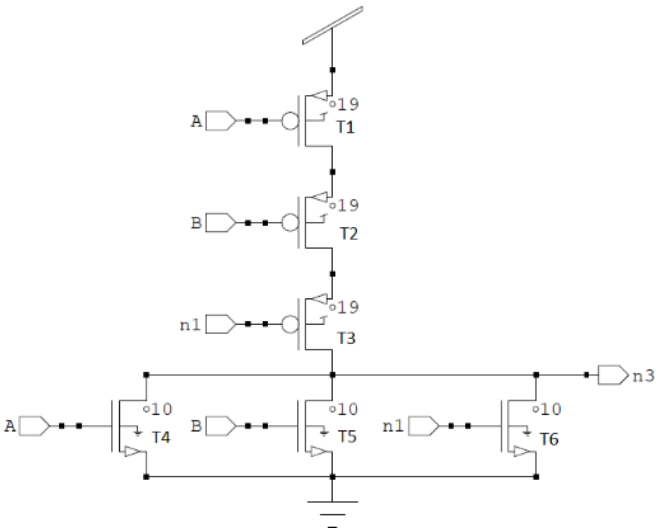

Fig. 4. The circuit can detect that the inputs are the same and equal to one

The design of the negative ternary NAND is shown in Fig. 2. In this figure, the chirality value of each transistor is written beside it.

In [20] positive ternary invertor is used to build a positive ternary NAND (PT-NAND). The output of this NAND will be zero if both of its inputs have the logic value of two. The design of this circuit is shown in Fig. 3.

Fig. 4, shows a circuit that its output will be the logic value two if both of its inputs have the logic value one. This circuit operates as follows:

If the inputs are smaller or equal to logical one, then the transistors T1 and T2 will be turned ON. The transistor T3 is connected to the negative ternary NAND output, therefore it will be turned ON when none of the inputs are zero. In the other words, the power supply could be reached in output when both of the inputs are equal to a logical one.

The truth table of all of the described circuits, that are used on the main body of multiplier-circuits, are shown in Table 4.

A	B	N1	N2	Not N2	N3
0	0	2	2	0	0
0	1	2	2	0	0
0	2	2	2	0	0
1	0	2	2	0	0
1	1	0	2	0	2
1	2	0	2	0	0
2	0	2	2	0	0
2	1	0	2	0	0
2	2	0	0	2	0

Table 4. The truth table of the circuits that are used on the main body of multipliers

The main body of the first proposed multiplier circuit is based on CMOS and it is shown in Fig. 5. In this design, the negative ternary NAND is connected to the T1, T4, also the inverted output of positive ternary NAND is connected to the T2 transistor. The output of the circuit that can detect the inputs are the same and equal to one, is connected to the T3 transistor. This circuit works as bellows:

If any of the inputs is logical zero, then only the T4 transistor will be turned ON and then the output of the multiplier circuit will be zero. If none of the inputs are zero, then the transistor T1 will be turned ON.

If both of the inputs are equal to one, then the transistors T1 and T3 will be turned ON to make logical one on the output.

If both of the inputs are logical two, then the transistors T1 and T2 will be turned ON to make logical one on the output.

Only the T1 transistor will be turned ON if one of the inputs is the logical one and the other is logical two. In this case, the output equals the logical two.

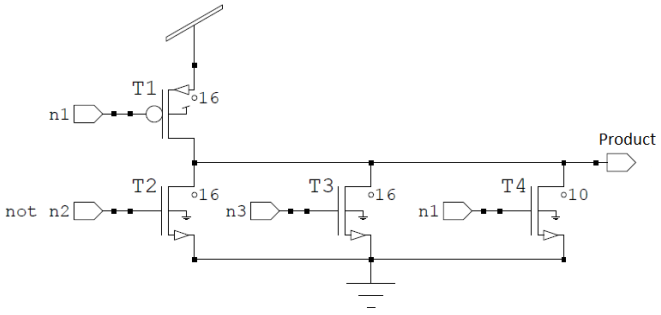

Fig. 5. First proposed ternary multiplier main body

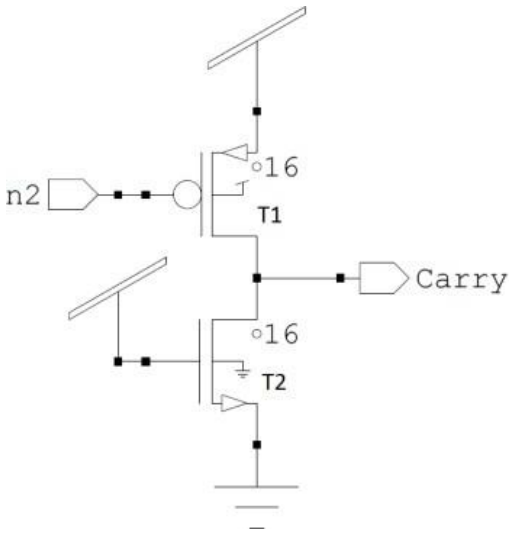

Fig. 6. The Carry circuit of the first ternary multiplier

The design of the carry circuit is shown in Fig. 6. The carry of ternary multiplier circuit will be a logical one just when both of the inputs are equal to two. In the other cases, it will be zero. To this fact, the transistor T2 is connected to the Vdd and always is ON, the T1 transistor is connected to the positive ternary NAND output to make the transistor ON just when both of the inputs are equal to logical two.

The main body of the second proposed multiplier is shown in Fig. 7. This circuit is made with a combination of switching and pass-transistor logic (PTL). Negative ternary NAND output is connected to T1 and positive ternary NAND output is connected to T8 and T10 transistors. If one of the inputs be zero then the output will be zero by the T1 transistor. If one of the inputs be one then the other input will send to the output. For example, if A=1 then T3, T2 and T4 will be ON and the B-value will be transmitted to the output. If both of the inputs equal to the logical two then T8 and T10 transistors will be turned ON and a logical one will be on the output by the T9 and T10 transistors.

The carry circuit of the second proposed multiplier is shown in Fig. 8. This circuit consists of two NCNFET transistors and two PCNFET transistors. Positive ternary NAND output is connected to the T2, T1, T3 transistors. The gate of the T4 transistor is connected to the power supply. If both of the inputs are not equal logical two then the output will be zero by the T1 transistor, else a logical one will be created in the output by T4, T2, and T3 transistors.

The second proposed multiplier has less power consumption than the first multiplier. The experimental results show that this power consumption reduction is due to the ground connection of the source of the PCNFET and the connection of the source of the NCNFET to the voltage source in order to produce a logical one.

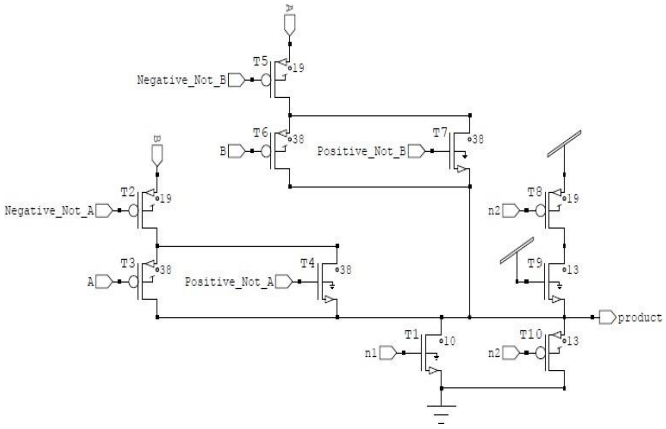

Fig. 7. Second proposed ternary multiplier main body

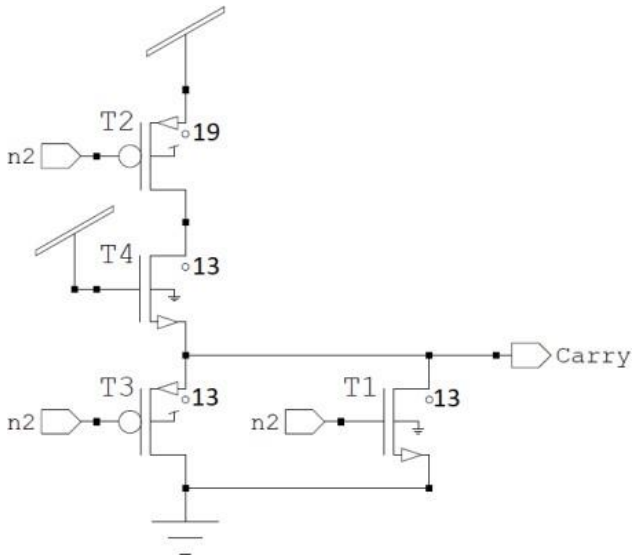

Fig. 8. The Carry circuit of the second ternary multiplier

5. Simulation Results

In this section, the proposed multipliers are compared with the multipliers from [10], [17] and [21] because all of these multipliers are designed by CNFET technology and operated in radix three.

The waveform of the input signals is shown in Fig.9. Fig. 10 and Fig. 11 show the first and the second multiplier transient response respectively to validate their operation.

All the circuits are simulated by Synopsys HSPICE 2014 with the CNFET library [22], 0.9-volt power supply, 250 MHz frequency, 32 nm nanotubes length, and 1fF load capacitor on the output. Some of the most important simulation parameters are shown in Table 5.

Comparison of the multiplier circuits is shown in Table 6. This comparison is done according to the number of transistors, delay, power consumption, and PDP. Moreover, the performance of the multipliers is examined by varying the load capacitance of the output in the range of 0 to 5 femtoFarad. The diagram for this examination is shown in Figures 12, 13, 14.

Parameters	Briefly Description	Quantity
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
EFI	The Fermi level of the doped S/D tube	6 eV

Table 5. The CNFET model parameters

According to Table 6, it's obvious that the first proposed design has the lowest number of transistors in comparison with the others, while its latency is slightly more than the fastest circuits. However according to the diagram of Fig. 12, it is clear that this circuit has better stability against the load capacity changing than the other circuits.

	# of Transistor	Delay (e-11)	Power (e-6)	PDP (e-17)
Frequency = 250 MHz, Load = 1 fF, $Vdd = 0.9v$				
Proposed 1	22	2.0068	15.221	30.545
Proposed 2	30	1.6335	0.2014	0.32898
Design of [17]	34	3.4311	0.24065	0.8257
Design of [10]	32	4.9163	0.14811	0.72816
Design of [21]	26	1.67	58.794	98.189
Frequency = 100 MHz, Load = 1fF, $Vdd = 0.9v$				
Proposed 1	22	1.9704	13.373	26.351
Proposed 2	30	1.5876	0.15991	0.25387
Design of [17]	34	3.3813	0.1882	0.63635
Design of [10]	32	4.9261	0.10994	0.54158
Design of [21]	26	1.709	57.133	97.639

Table 6 The simulation results of the ternary multipliers

According to the simulation results, it's clear that the second proposed design is the fastest circuit among the ternary multipliers and also has least power consumption than the other designs except for the design of [10]. Whereas, it should be note that the design of [10] made a logical one by the power supply, instead of making it with the entire circuit. The second proposed design has the least PDP compared to other multipliers while the number of transistors that are used in this design is just 30 which is less than a lot of the multipliers [11], [5] and [10], [17].

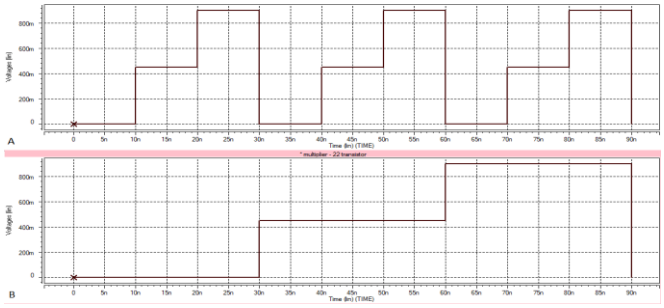

Fig. 9. The input signals for the multiplier circuits

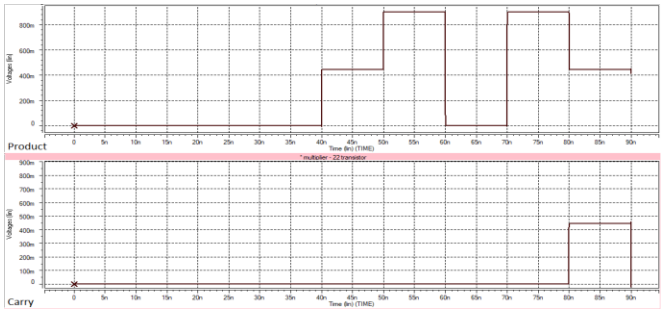

Fig. 10. The outputs of the first proposed ternary multiplier

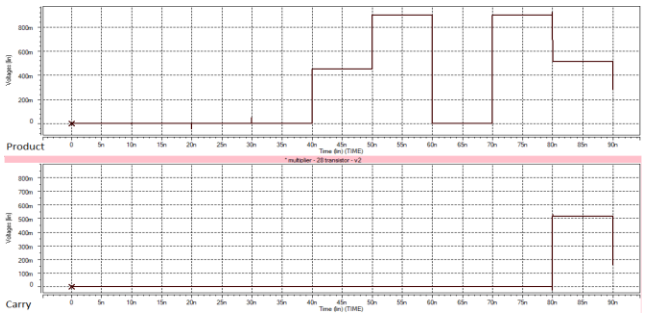

Fig. 11. The outputs of the second proposed ternary multiplier

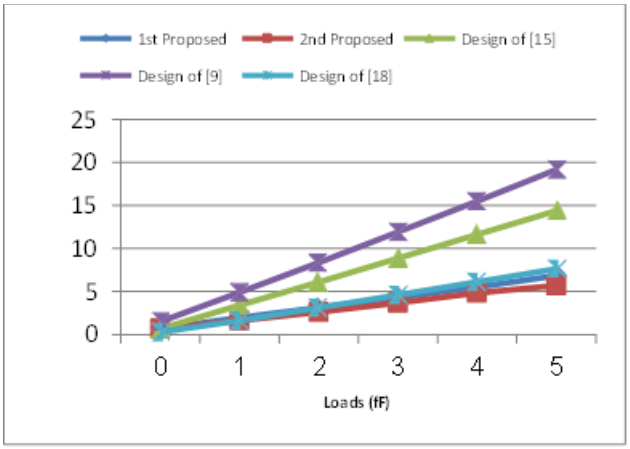

Fig. 12. The delay of the multipliers VS their output's load capacitance

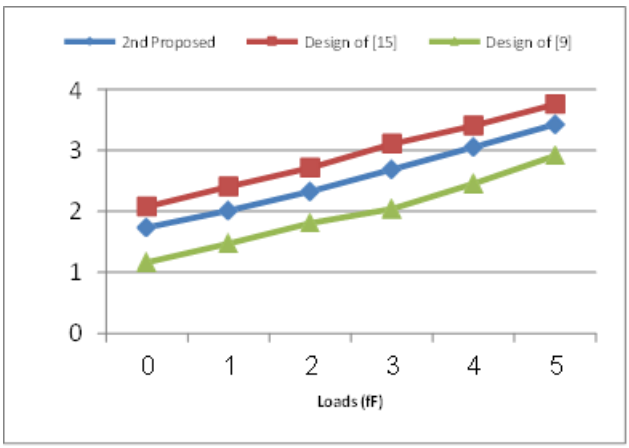

Fig. 13. Power consumption of the multipliers VS their output's load capacitance

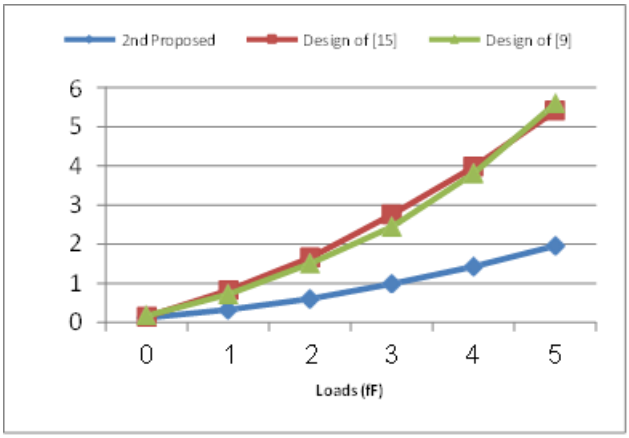

Fig. 14. The PDP of the multipliers VS their output's load capacitance

6. Conclusion

Reducing the size and increasing the efficiency of the multipliers lead to increasing the speed and reducing the power consumption of a computation circuit, because they are one of the basic computation operations in many computation systems.

In this paper, two ternary multipliers are proposed. The first multiplier is based on CMOS and the other is based on a combination of pass-transistors, and transmission gates.

The first proposed multiplier not only has a short delay but also it has the lowest number of transistors among the multipliers. The second proposed multiplier is the fastest one between the compared multipliers. Also, it has the least power consumption among all the multipliers those have only one power supply to develop all the required logical levels. Furthermore, the second proposed design has few numbers of transistors and also it has the lowest power delay product (PDP).

All the considered multiplier circuits, in this paper, are simulated by HSPICE simulator with CNFET library.

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