The CSI Journal on Computer Science and Engineering

Journal homepage: www.csionjcse.ir

Automatic Analog IC Layout with CNN-Based Placement Using SqueezeNet and Multi-Objective Routing via DE and NSGA-III

Mehdi Gholamian Salahi[1], Hadi Dehbovid[2*], Mehdi Radmehr[1], Seyed Mahmoud Anisheh[1]

[1] Department of Electrical Engineering, Sari Branch, Islamic Azad University, Sari, Iran
[2] Department of Electrical Engineering, Nour Branch, Islamic Azad University, Nour, Iran

*** Corresponding author email address**: hadi.dehbovid@gmail.com

A r t i c l e I n f o

Article type:
Original Research

How to cite this article:
Gholamian Salahi, M., Dehbovid, H., Radmehr, M., & Anisheh, S. M. (2026). Automatic Analog IC Layout with CNN-Based Placement Using SqueezeNet and Multi-Objective Routing via DE and NSGA-III. *The CSI Journal on Computer Science and Engineering, 20*(2), 24-37.
http://dx.doi.org/10.22034/jcse.2026.572666.1075

A B S T R A C T

The layout design of analog integrated circuits (ICs) is a challenging and time-consuming task, requiring manual effort to extract geometric constraints such as symmetry and proximity. This paper presents a novel approach for automatic layout generation, com-bining the power of convolutional neural networks (CNNs) with transfer learning, specifically using the pre-trained SqueezeNet mod-el to extract these constraints from schematic images. By applying fine-tuning, the CNN model can effectively identify and extract the necessary geometric relationships, eliminating the need for manual extraction. For the routing process, a multi-objective optimiza-tion strategy is employed using the non-dominated sorting genetic algorithm III (NSGA-III), where wire length, via count, and arch segments are minimized. To address the challenge of generating an effective initial population for NSGA-III, we introduce the differ-ential evolution (DE) algorithm as a method for generating high-quality initial solutions, enhancing the convergence speed and solu-tion quality. The proposed methodology is applied to the layout design of a two-stage operational amplifier (op-amp), with simula-tions conducted using MATLAB and validated in Cadence software on a 0.18µm CMOS process at a 1.8 V supply voltage. The results show that the proposed method significantly outperforms existing techniques in terms of layout efficiency, performance, and auto-mation in the design process.

Keywords: *Symmetry and proximity, Transfer learning, SqueezeNet, Routing, DE-NSGA-III.*

Article history:
Published online 07 August 2026

1 Introduction

Analog circuit design is a fundamental aspect of electronics engineering, with applications in many modern electronic devices. These circuits are responsible for processing analog signals and converting them into usable information for digital systems or vice versa. Routing in analog integrated circuits (ICs) is also a crucial process in circuit design, as it significantly impacts the final circuit performance, including power consumption, speed, and signal quality [1-4]. Accurate routing ensures reduced electromagnetic interference and enhances system stability and efficiency. Therefore, precise and optimal analog circuit design and routing are essential for achieving desired performance in electronic systems. Analog circuit design faces several challenges, some of which are related to the geometric and physical complexities of the circuit. One of the primary problems is the accurate extraction of geometric constraints such as symmetry and proximity, which require high precision and complex analysis. Additionally, the routing process in analog circuits presents challenges such as minimizing wire length, reducing the number of vias, and optimizing bends, all of which impact the circuit's efficiency and cost. Furthermore, parasitic effects caused by suboptimal routing or inaccurate design can significantly degrade the performance of analog circuits, necessitating more precise design control [5-8].

In the complex and challenging world of analog circuit design, the use of Electronic Design Automation (EDA) tools has become essential. These tools significantly help designers by accelerating the design process and providing higher accuracy in circuit simulation and optimization. The use of EDA not only reduces design time but also enables the simulation and correction of design issues before fabrication, which significantly lowers potential risks and costs [9-11]. Moreover, EDA tools allow designers to use real data and more accurate models for simulation. These simulations help designers predict circuit behavior under various operational conditions, allowing them to address issues such as noise, signal degradation, and power or thermal problems before physical components are produced. On the other hand, EDA tools also assist in design optimization. For example, using automatic optimization algorithms, these tools can generate designs with the best performance and lowest possible cost. As a result, manufacturing costs are reduced, and circuit performance is improved compared to traditional methods.

Neural networks, especially deep neural networks (DNNs), are powerful tools for the automatic extraction of complex features and geometric constraints in analog circuit design. These networks can accurately identify and extract various geometric constraints such as symmetry, proximity, and other critical constraints in circuit design. In traditional methods, this process is done manually by designers, which is not only time-consuming but also prone to errors. However, by using neural networks, the feature extraction process is automated, leading to faster and more accurate designs [12-14].

In this context, one widely used model is Transfer Learning, which utilizes pre-trained models for identifying geometric features. For example, models like SqueezeNet, which have been trained on large datasets, can recognize the geometric features of analog circuits in schematic images. These models can directly extract features from input data and identify geometric constraints that are essential for later stages of the design process, such as routing. Since these models continually learn from data, they can significantly improve the accuracy and speed of feature extraction, relieving designers from performing manual and time-consuming steps. These techniques, especially in the design of complex and large-scale circuits, where accurate extraction of geometric constraints and features is crucial, can be extremely valuable. The use of neural networks for feature and geometric constraint extraction not only increases the accuracy of designs but also reduces design time, accelerating the overall process of analog circuit design [15-17].

Evolutionary algorithms, especially Non-dominated Sorting Genetic Algorithm III (NSGA-III), are effective methods for optimizing the routing process in analog circuits. These algorithms are capable of optimizing multiple objectives simultaneously, which is crucial in analog circuit routing. For instance, the main goals in analog circuit routing are to minimize wire length, the number of vias, and the number of bends [15-17]. The NSGA-III algorithm can optimize these objectives simultaneously by using populations of solutions generated through the evolutionary process. Since routing in analog circuits is accompanied by various challenges, these algorithms help in finding the most effective solutions to achieve better circuit performance.

In the routing process of analog circuits, several fundamental challenges must be addressed by designers. One challenge is minimizing the wire length. Long wires can lead to increased parasitics, signal interference, and higher

power consumption. Therefore, the routing design must be optimized to minimize wire length. Another challenge is minimizing the number of vias, which are vertical connections between different layers of the circuit. Excessive use of vias can reduce speed and increase manufacturing costs. Additionally, minimizing the number of bends is also a critical challenge, as each bend can increase resistance and inductance in the circuit, potentially leading to poorer performance. Evolutionary algorithms like NSGA-III can effectively handle these challenges during the optimization process, ensuring the best balance between these parameters. The remainder of the paper is organized as follows: the existing methods are presented in Section II, the proposed method is introduced in Section III, simulations are described in Section IV, and the conclusion is given in Section V.

2 Related Works

The literature provides several methods for generating layouts of integrated circuits [15-25]. The paper [17] introduces an automated placement and routing technique for generating the layout of CMOS operational amplifiers (op-amps). Unlike traditional methods, the proposed approach incorporates layout effects directly during the generation phase. A new layout generator is used to extract parasitic and geometric information, ensuring more accurate performance estimation. To handle the optimization process, a multi-objective evolutionary algorithm based on decomposition (MOEA/D) is employed. However, a key limitation of this approach is the manual extraction and specification of design constraints, which can reduce efficiency and limit scalability in fully automated design flows.

The study [15] introduces a new placement and routing approach for analog integrated circuit layout generation, utilizing a modified version of the cuckoo optimization algorithm (COA). To preserve circuit performance, the method incorporates layout parasitic effects during the design process. A key drawback of this approach is the randomness of the initial routing solutions, which may lead to suboptimal performance in certain cases.

The paper [16] introduces a heuristic method for placing analog and mixed-signal integrated circuits. The focus is on analog placement, specifically addressing features like distance constraints between devices. The problem is formulated using integer linear programming, and a priority-driven constructive heuristic is proposed, drawing from algorithms used in the facility layout problem. The approach minimizes the perimeter of the circuit's bounding box and the length of the wiring, while considering various device variants. Key constraints, such as symmetry and blockage areas, are also incorporated. The method is validated on both synthetic and real-world industrial cases, using genetic algorithms and covariance matrix adaptation evolution strategy for optimization, along with reinforcement learning for hyperparameter tuning. The layout design of analog and mixed-signal (AMS) integrated circuits differs markedly from digital ICs due to the diversity and complexity of their components. AMS layouts often include a broad spectrum of elements and may integrate pre-designed subcircuits, especially in hierarchical systems. Because these components can occupy various fabrication layers, effective device placement requires coordinated optimization during the layout process to achieve desired circuit performance. Importantly, some components can be placed on mutually exclusive layers, enabling deliberate overlap in their layout. This strategy helps reduce total chip area and interconnect length without compromising performance. In [21], an analytical framework is proposed to solve the analog placement problem while accounting for layer-specific constraints.

The paper [18] introduces a new placement process where different placements with varying aspect ratios are generated for each block. The solutions are selected based on minimizing the area. The results are validated through post-layout simulations to ensure that the final placement satisfies the target specifications. In [20], a machine learning technique for analog IC placement is proposed. Simulation results for several amplifiers demonstrate that the approach achieves performance comparable to manual design while maintaining high speed. The paper [19] presents an innovative method for analog IC placement utilizing an artificial neural network (ANN). A loss function is applied to the model to generate optimal placements. The performance of this method was evaluated using a trained ANN for two-stage amplifiers.

The paper [24] presents an analog layout placement and routing flow using device unit elements. Device placement is achieved with Satisfiability Modulo Theories (SMT) techniques, and routing is handled by a procedural router. The placer tool generates multiple layouts that meet constraints, while a routing channel estimator calculates the area needed for each solution, considering matched groups and net currents. This approach allows for a more realistic

selection of the optimal layout based on system aspect ratio and area constraints. The proposed approach in [25] presents a semi-automated analog placement method, allowing designers to maintain control while benefiting from automation in specific tasks. This method adopts a row-based organizational structure, which is common in digital circuit design, and adapts it to analog layouts. The row-based approach helps streamline the placement process by organizing components in distinct rows, providing a clear and efficient framework for device positioning. Although the process is automated to assist with repetitive tasks, the designer is still involved in key decisions, ensuring that the specific requirements and performance constraints of the analog circuit are met. This combination of designer oversight and automation offers a balance between efficiency and flexibility, improving the overall design flow while maintaining high customization and precision.

In [22], a dedicated graph neural network model is developed to predict the impact of placement on circuit performance. The knowledge obtained from this model can be utilized across different topologies within the same circuit type. In [23], a comprehensive analysis of analytical techniques for analog placement is provided. The proposed approach outperforms simulated annealing in terms of circuit performance, area efficiency, and runtime for performance-driven placement.

3 Proposed Method

The layout design process of analog ICs presents persistent challenges such as manual extraction of geometric constraints, complex routing, and achieving optimal performance. This study proposes an automated and intelligent framework for layout generation, which comprises three main stages: geometric constraint extraction using convolutional neural networks (CNNs) [26-30], component routing via multi-objective optimization with NSGA-III [31, 32], and initial population generation using the Differential Evolution (DE) algorithm [33, 34]. Flowchart of the proposed method is shown in Figure 1.

In the first stage, a schematic image of the circuit is used as input to the SqueezeNet model. Through transfer learning and fine-tuning, the network becomes capable of identifying features such as symmetry and proximity among circuit elements. The output of this stage is a set of geometric constraints that are passed to the routing process.

In the second stage, the routing problem is formulated as a multi-objective optimization task, with objectives including minimization of wire length, number of vias, and number of routing bends. To solve this problem, the NSGA-III algorithm is employed, which maintains diversity in the solution set and applies non-dominated sorting to produce efficient and varied solutions.

Finally, to enhance the quality of the initial solution set and improve the convergence speed of NSGA-III, the DE algorithm is used to generate a high-quality initial population. By combining these three key modules, the proposed framework performs layout design with high accuracy, speed, and a significant degree of automation, outperforming traditional methods in both efficiency and performance.

3.1 Geometric Constraint Extraction using CNN and Transfer Learning

In analog integrated circuit layout design, geometric constraints such as symmetry and proximity play a critical role in improving electrical performance and minimizing noise. These constraints are traditionally extracted manually by designers, which is both time-consuming and error-prone. In the proposed method, an intelligent deep learning-based approach is introduced to automatically extract these constraints from schematic images.

To achieve this, the SqueezeNet model is employed as a lightweight and efficient convolutional neural network (CNN). SqueezeNet is pre-trained on general image datasets such as ImageNet and is capable of extracting high-level features from input images. Through transfer learning and fine-tuning, the network is adapted to recognize specific features within analog circuit schematics.

During the fine-tuning phase, the final layers of the network are retrained using a dataset composed of

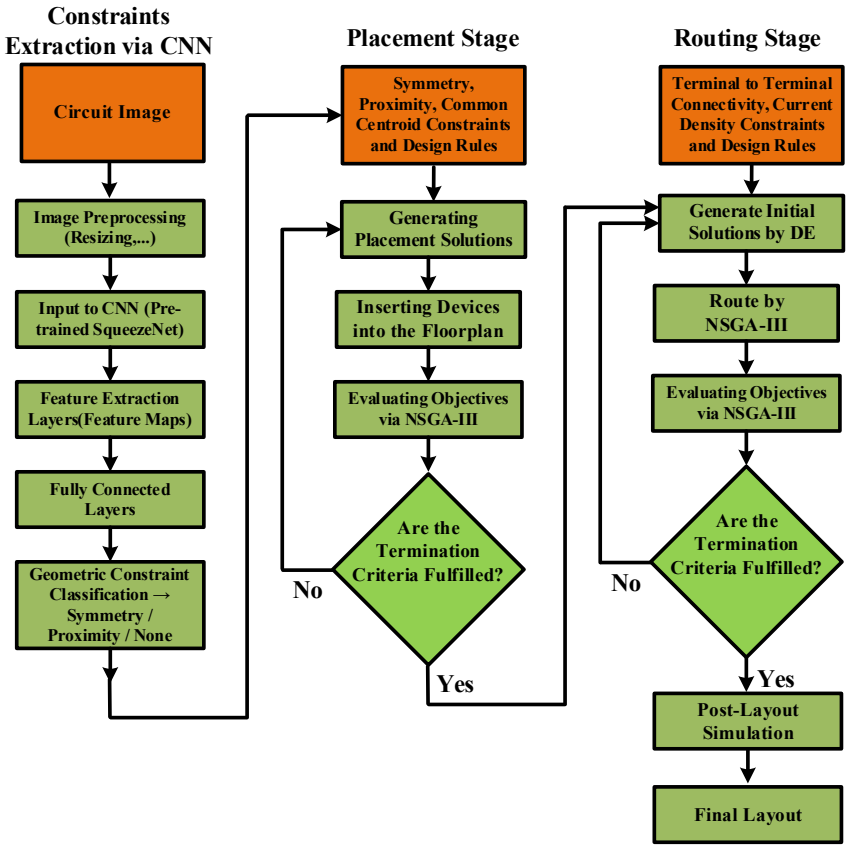


Figure 1: Flowchart of the proposed method.

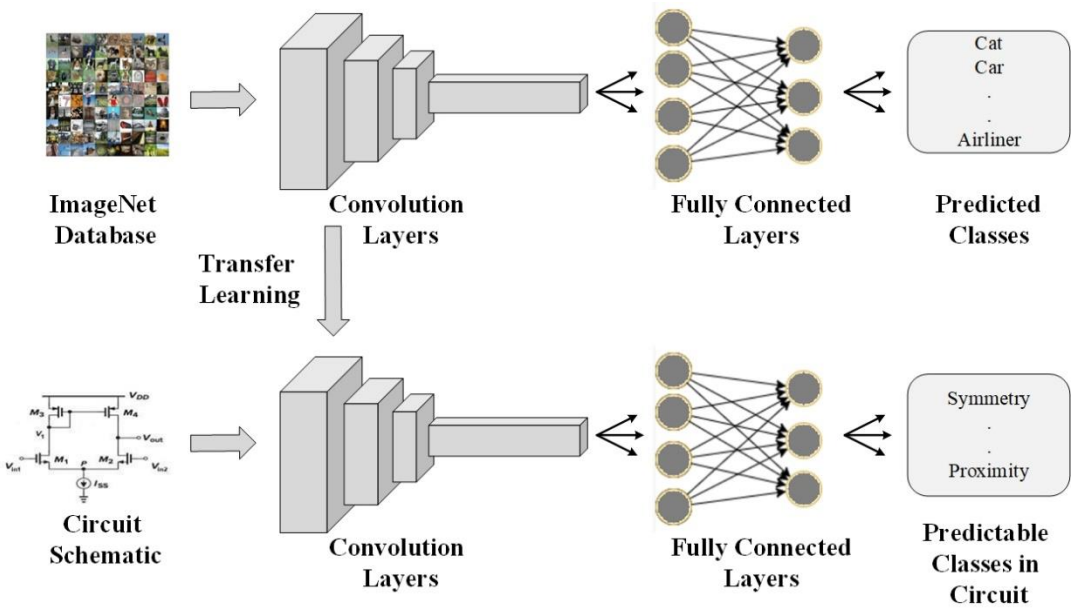


Figure 2: Constraints Extraction using CNN and Transfer Learning.

Schematic diagrams, enabling the model to learn meaningful relationships between transistors, current paths, and structural patterns such as symmetry and proximity. The output of this process is a feature map that includes labeled regions exhibiting symmetry and close proximity among circuit components. These extracted constraints are then passed on to guide the routing and optimization stages of layout generation. This architecture is shown in Figure 2.

3.2 Layout Representation and Encoding

For optimization in the analog circuit layout design process, accurate and efficient component placement is crucial. In order to apply optimization algorithms such as NSGA-III, it is necessary to represent and encode the placement of components in a way that captures the geometric and structural relationships between the elements. In this study, to simplify and facilitate the application of optimization algorithms, the bottom-left corner coordinates of each component are used as the reference for defining the position of each element in the design space. These coordinates directly specify the location of each component relative to the global coordinate system of the layout.

Each circuit component, including transistors, resistors, capacitors, and other elements, is considered as a simple rectangle, with its position defined by the (x, y) coordinates of its bottom-left corner. These coordinates are then used as the primary features in the optimization algorithms to determine the optimal location for each component. In the encoding stage, these coordinates are placed into a gene string that represents the position of each component in the design space. For example, for a circuit consisting of N components, the gene string contains N pairs of (x, y) coordinates, each pair representing the bottom-left corner of a component. This gene string is then provided as input to the optimization algorithm, which attempts to optimize the placements based on objective criteria such as geometric balance. This method of representation and encoding allows for effective and efficient optimization using evolutionary algorithms such as NSGA-III and other optimization techniques.

3.3 Initial Population Generation via Differential Evolution

In evolutionary algorithms, selecting a high-quality initial population is crucial, as it significantly affects the convergence speed and the final solution quality. In this study, the DE algorithm is used effectively to generate a high-quality initial population for the NSGA-III algorithm. The DE algorithm is typically used for optimizing complex and multi-objective problems. In this approach, the DE algorithm is employed to generate a set of diverse and high-quality initial solutions that can be used as input to NSGA-III. This method helps improve the convergence speed and the quality of the final results.

Initially, a set of random initial solutions is generated using DE. In this process, the DE algorithm creates multiple initial solutions, where each solution (or chromosome) is a gene string that includes the location of segments for wiring in the circuit. Then, through mutation and crossover operations, the initial population continuously moves towards optimal regions. During this process, DE operations such as the difference between two random solutions are used to update the population and generate new solutions. The generation of new populations is done in a way that preserves diversity throughout the process, potentially leading to better solutions for the circuit design problem.

The population created by DE is then input into the NSGA-III algorithm. At this stage, NSGA-III uses non-dominated sorting and population diversity to perform multi-objective optimization and generate better solutions. The use of DE in this stage increases initial population diversity and improves solution quality, ultimately leading to faster convergence and better results in the NSGA-III algorithm. This combination of DE and NSGA-III enhances the efficiency of the optimization process and improves the accuracy of the analog circuit layout design.

3.4 Multi-objective Optimization using NSGA-III

In the optimization process of analog circuit layout design, objective functions play a key role in evaluating and comparing the quality of solutions. These objective functions typically include the following:

1. Wire Length: This objective function refers to the total length of the wires used in the circuit. The goal is to minimize the wire length to prevent unnecessary energy consumption and wasted space while maintaining the circuit's performance.
2. Number of Vias: This objective function refers to the number of vias connecting different layers of the circuit. Using fewer vias is desirable as vias increase energy consumption and manufacturing costs.
3. Number of Bends: This objective function refers to the number of bends in the wiring. Simpler designs with fewer bends are generally more cost-effective and efficient.

These objective functions are considered multi-objective in the optimization process, meaning they should all be minimized simultaneously.

Non-dominated sorting is a crucial step in multi-objective optimization algorithms like NSGA-III. In this process, all population members are sorted using the concept of non-dominance. A solution is considered non-dominated if no

other solution in the population is better than it in all objective functions. In other words, a solution that is not worse than any other solution in all objective functions is classified as a non-dominated solution. Once the non-dominance of solutions is determined, these solutions are placed in sorting layers and ranked from best to worst. This ranking allows the algorithm to select higher-quality solutions in the selection process and subsequent generations.

Mutation and crossover are essential operations in evolutionary algorithms that are used to generate new populations.

1. Mutation: In the mutation operation, a random change is made to a selected solution to maintain diversity within the population. This change could include shifting the coordinates of one or more circuit elements, altering wire connections, or making minor changes in the wiring structure. This operation helps the algorithm efficiently escape local optima.
2. Crossover: The crossover operation generates new solutions by combining two parent solutions (chromosomes). In this operation, sections of the parent solutions are swapped to create a new generation of solutions that incorporates features from both parents. This operation promotes information exchange between solutions and broadens the search space.

Ultimately, by using mutation and crossover, a new population is generated that is more diverse and of higher quality, which is then provided to the algorithm for evaluation and selection in subsequent generations.

3.5 Routing Strategy and Layout Construction

The routing algorithm plays a crucial role in the layout design of analog integrated circuits by determining the paths for interconnecting various components of the circuit. This process is carried out alongside the extracted constraints, including symmetry, proximity, and balance, to ensure that the design meets the desired specifications. The routing process can be broken down into the following steps:

1. Routing Algorithm: The routing algorithm is designed to find the optimal path for connecting the circuit components while minimizing the predefined objective functions such as wire length, via count, and bend count. The algorithm works by iteratively selecting the most optimal paths for the connections between circuit nodes (components) while adhering to the geometric constraints extracted from the schematic images. These constraints help ensure that routing paths do not violate design rules such as symmetry and proximity.
2. Node Connection Logic Based on Extracted Constraints: The connection logic between nodes is determined based on the constraints extracted during the schematic analysis phase. These constraints include:
    - Symmetry: Ensuring that nodes that need to be symmetrically placed are properly connected to maintain balanced routing paths.
    - Proximity: Nodes that need to be placed near each other are connected first to minimize routing distance.
    - Balance: Ensuring that wiring is done in a balanced way to avoid long or overly complex routing paths.

The routing algorithm uses this logic to establish a set of connections that respect these constraints while also minimizing wire length and via count.

3. Conversion of Optimized Solutions to Executable Layout in Cadence: Once the routing process has been completed and the layout optimized, the resulting solution must be converted into a format that is compatible with Cadence for actual implementation. In this stage, all DRC (Design Rule Check) rules are implemented in MATLAB. The resulting layout is then carefully compared with the DRC rules to ensure that all design conditions and constraints are met. After this verification in MATLAB, the layout is transferred to the Cadence environment for final verification.

4 Simulation Results

Experimental evaluations were conducted using MATLAB R2021b on a system equipped with an Intel® Core™ i7-6700K processor (4 GHz) and 32 GB of RAM. The NSGA-III algorithm was employed, configured with a population size of 100 and executed over 100 generations. In this study, transfer

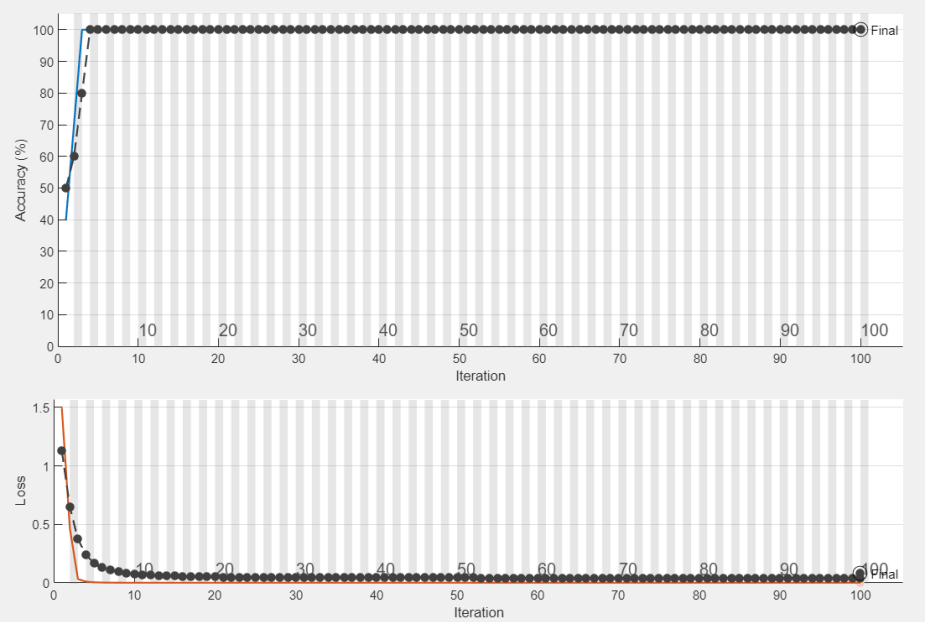


Figure 3: Training Process of the Customized SqueezeNet Model.

Learning based on the SqueezeNet convolutional neural network was employed to automatically extract geometric constraints from circuit schematics and classify them accordingly. The image dataset, consisting of categorized schematic diagrams, was loaded using MATLAB's imageDatastore. The dataset consists of 512 analog circuit schematic images, collected from published literatures [35-41] and complemented with synthetically generated and modified schematics. The synthetic samples were created by rearranging device placements, orientations, and interconnections while preserving functional correctness and geometric constraints.

Since SqueezeNet requires input images of size 227×227×3, all images were converted to RGB and resized appropriately using the augmentedImageDatastore utility. Minimal data augmentation was applied to preserve the structural integrity of the schematics, including slight translations, scaling, and minor variations in line thickness. These preprocessing and augmentation steps ensured robust training of the CNN model while maintaining accurate representation of geometric constraints.

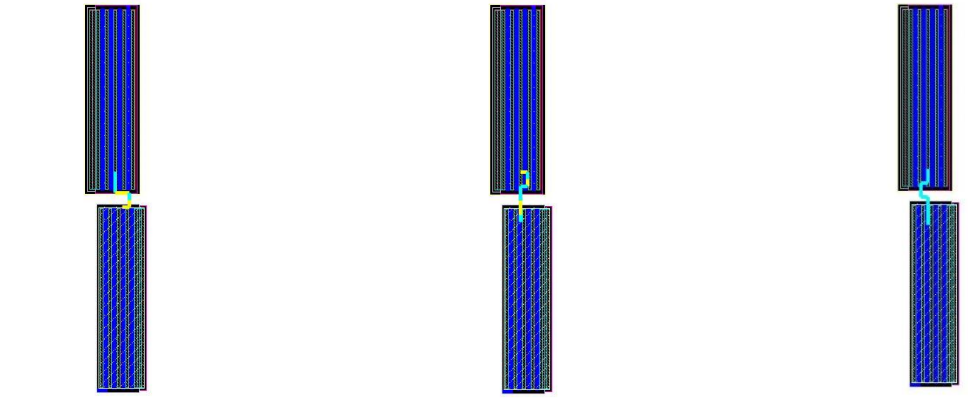
The original SqueezeNet architecture was customized by modifying its final layers to match the number of classes in the dataset. Specifically, the fully connected, softmax, and classification layers were replaced. The number of classes corresponds to the distinct geometric constraint categories considered in the layout generation process. Each class represents a specific geometric relationship extracted from schematic diagrams, such as: Symmetry constraints (e.g., differential pairs, current mirrors) Proximity constraints (e.g., closely coupled devices for matching) The final classification layers of the SqueezeNet model were modified to match the total number of these predefined constraint classes.

The training process was performed using the stochastic gradient descent with momentum (SGDM) optimizer over 100 epochs with an initial learning rate of 0.01. A piecewise learning rate schedule was implemented to improve convergence, and validation was carried out on the test set at regular intervals.

The dataset was randomly partitioned into three subsets to enable robust training and fair performance evaluation. Specifically, 70% of the data was used for training, 15% for validation to fine-tune model hyperparameters and prevent overfitting, and the remaining 15% was reserved for testing to assess the model performance on unseen schematic images. This splitting strategy ensures a reliable evaluation of the proposed method for analog IC layout generation. Figure 3 illustrates the training process of the customized SqueezeNet model in terms of classification accuracy and loss. As shown in the accuracy curve, the model rapidly improves during the initial epochs and gradually converges to a high accuracy of approximately 99.8% on the validation set. Simultaneously, the training and validation loss curves exhibit a steady decline, indicating that the model effectively minimizes the error without overfitting. The use of a piecewise learning rate schedule contributes to the smooth convergence and performance stability during training.

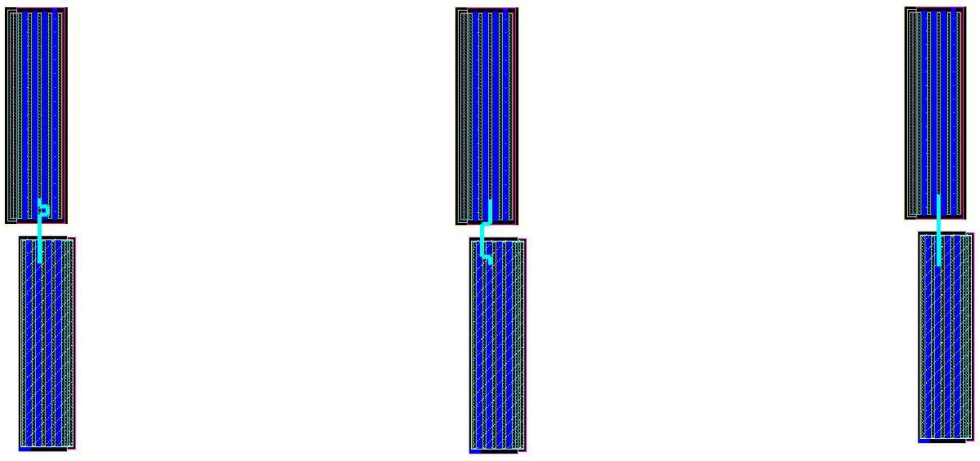
These results confirm that the proposed model learns meaningful visual features associated with geometric constraints from the schematic images.

To assess the effectiveness of the proposed routing optimization strategy, two simulations have been shown between two terminals: one utilizing the standard NSGA-III algorithm alone as shown in Figure 4, and the other incorporating a DE-based initialization for the NSGA-III population (Figure 5). The routing objectives included minimizing wire length, reducing the number of via transitions between metal layers, and avoiding unnecessary arch-shaped wire segments. In these figures, the wire segments shown in cyan and yellow represent routing on metal layers 1 and 2, respectively. The experiment demonstrated that integrating DE significantly improved the optimization process. In the DE-assisted run, a better routing solution was achieved with fewer iterations compared to the standard approach. Specifically, the total wire length was shorter, and the number of inter-layer via transitions was noticeably reduced, indicating a more efficient layout. This improvement can be attributed to the higher-quality initial population generated by DE, which allowed NSGA-III to converge more rapidly toward optimal trade-offs across multiple objectives. These results confirm the utility of DE as a population seeding mechanism in multi-objective analog IC routing tasks, not only accelerating convergence but also enhancing the final layout quality in terms of performance and complexity.



(a) (b) (c)

Figure 4. Routing result between two terminals using NSGA-III without DE-based initialization. The solution shows longer wire paths and more via transitions between metal layers. Wiring process after (a) 1 iteration, (b) 10 iterations, (c) 20 iterations.



(a) (b) (c)

Figure 5. Improved routing result using DE-initialized NSGA-III. The final layout exhibits shorter wire length, fewer vias, and reduced routing complexity. Wiring process after (a) 1 iteration, (b) 10 iterations, (c) 20 iterations.

To evaluate the performance of the proposed placement and routing method, it was applied to a two-stage operational amplifier presented in [35], as illustrated in Figure 6. This amplifier topology is widely recognized for its fundamental role in analog and mixed-signal integrated circuits [15, 35-41]. In this OTA, the transconductance of the first stage is enhanced through the use of a super class-AB recycling folded cascode (SCRFC) architecture. Moreover, active load structures are employed to further improve the effective transconductance. The combined effect of increased transconductance and the adoption of a multi-path signal processing scheme results in a higher DC gain. The multi-path technique is applied to both amplification stages. Additionally, a nonlinear current mirror is utilized to increase the drive capability of the output stage.

The detailed dimensions and design specifications of the amplifier are summarized in Table 1. This table comprehensively reports the transistor channel width-to-length (W/L) ratios used in the design, along with the values of the passive compensation elements. These compensation parameters have been selected in accordance with the design guidelines and specifications provided in the [35]. This amplifier serves as a fundamental building block in analog and mixed-signal circuit design, making it an appropriate benchmark for assessing the effectiveness of the proposed methodology.

The resulting layout, automatically generated by the proposed methodology, is illustrated in Figure 7. The proposed framework effectively translates the extracted geometric constraints into an optimized physical layout without requiring manual intervention from the designer. By explicitly considering symmetry and proximity relationships during placement and routing, the generated layout maintains key analog design requirements. The final layout occupies a total silicon area of 0.021 mm², demonstrating a compact and area-efficient implementation. This compactness is achieved without compromising layout regularity or signal integrity, highlighting the capability of the proposed approach to produce high-quality analog IC layouts while significantly reducing design effort and improving automation efficiency. Different process layers are visualized using distinct colors to enhance clarity: Metal 1 is shown in cyan, Metal 2 in yellow. This color scheme facilitates better understanding of routing distribution, interconnections, and silicon utilization across the chip surface. The results demonstrate that the proposed method is capable of producing clean, dense, and high-quality layouts, which are highly desirable in analog integrated circuit design.

To validate the accuracy and reliability of the generated layout, post-layout simulations were conducted using Cadence tools. These simulations help ensure that the proposed placement and routing method not only generates a compact and DRC-clean layout, but also preserves the desired analog performance of the circuit. The frequency-domain behavior of the two-stage operational amplifier based on the proposed automatically generated layout is illustrated in Figure 8. The corresponding Bode plots clearly demonstrate the small-signal frequency response of the amplifier. As observed, the amplifier achieves a high low-frequency open-loop gain of approximately 93 dB, indicating strong amplification capability and effective gain enhancement through the proposed architecture and layout strategy. Furthermore, the unity-gain bandwidth is measured to be around 330 MHz, confirming that the generated layout preserves high-speed characteristics. This wide bandwidth highlights the suitability of the proposed layout methodology for broadband analog applications, while ensuring that layout parasitics do not significantly degrade the overall frequency performance of the amplifier. Moreover, the phase margin is approximately 60°, confirming that the amplifier is stable. These results validate that the proposed layout strategy is effective not only in terms of area efficiency but also in preserving the essential analog performance metrics.

Table 2 provides a comparative analysis between the post-layout simulation results of the proposed method and those reported in previous works [15, 17]. The comparison covers several key metrics, including the DC-gain of the operational amplifier, the execution time of the placement and routing algorithm, the total layout area, and the effective area utilization. As observed, the proposed method demonstrates superior performance across all evaluated aspects of layout generation. This improvement is primarily attributed to the ability of the proposed CNN-based method to automatically incorporate proximity and symmetry constraints, which are critical for analog layout quality. In contrast, the existing methods fail to explicitly extract or apply such layout-aware constraints, performance and area efficiency. Moreover, by incorporating a Differential Evolution algorithm during the initial stage of the routing process, the proposed method is able to generate feasible solutions more rapidly. This evolutionary-based initialization provides the routing algorithm with a more

optimized starting population, which significantly enhances the convergence speed and overall efficiency of the layout generation process.

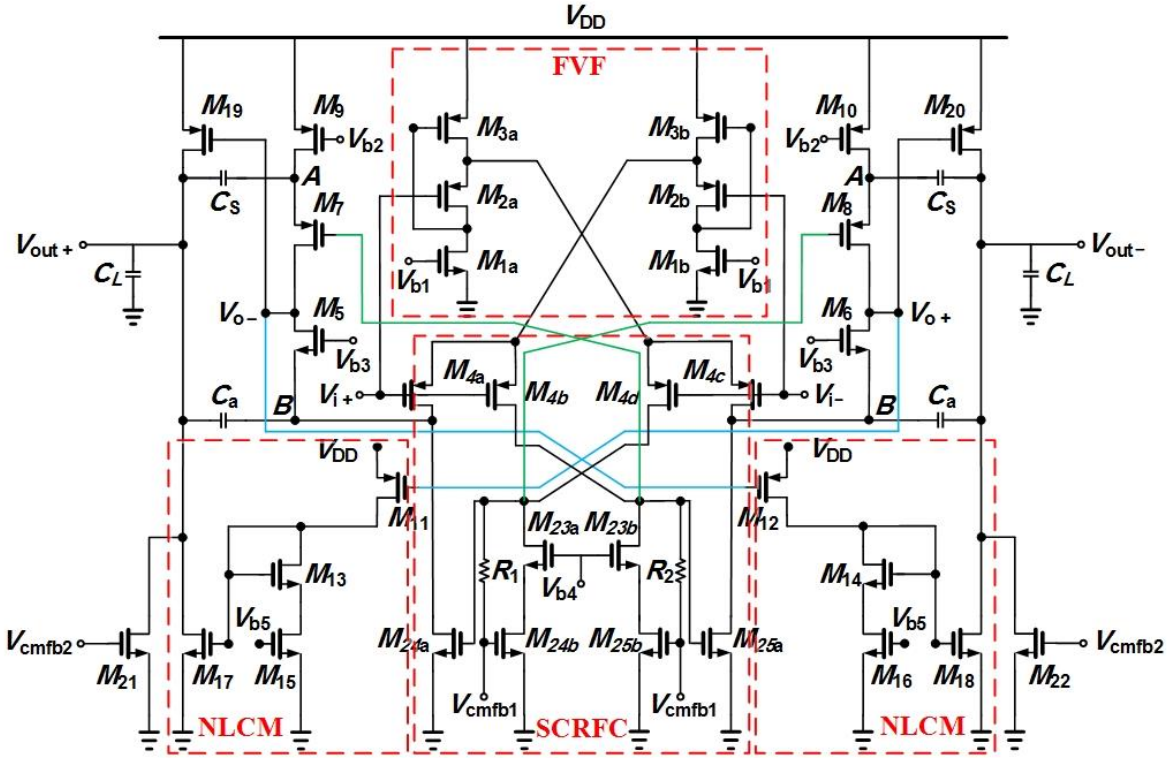


Figure 6. The proposed op-amp in [35].

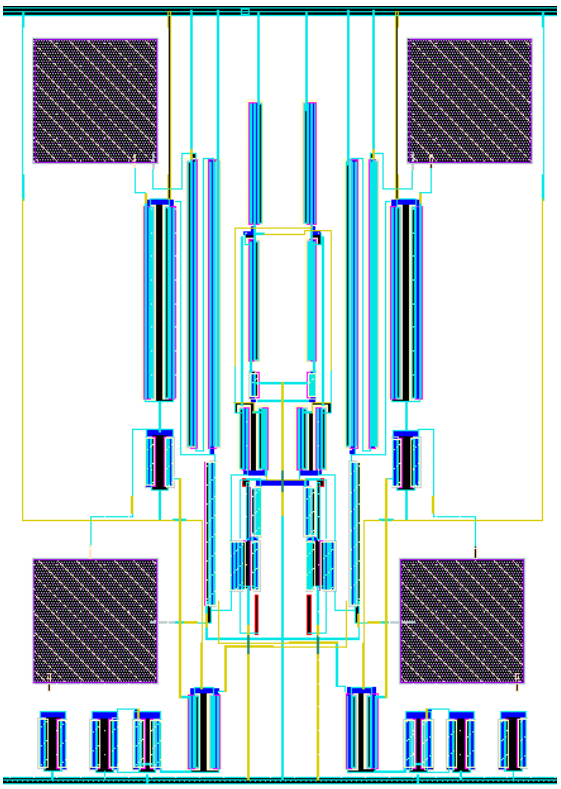


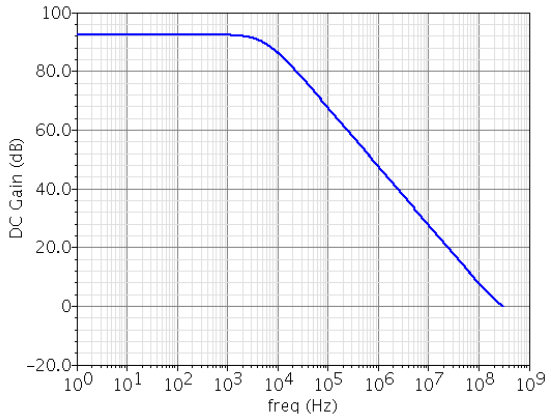
Figure 7: The resulting layout generated by applying the proposed algorithm.

Table 1: Values of the two-stage op-amp elements [35].

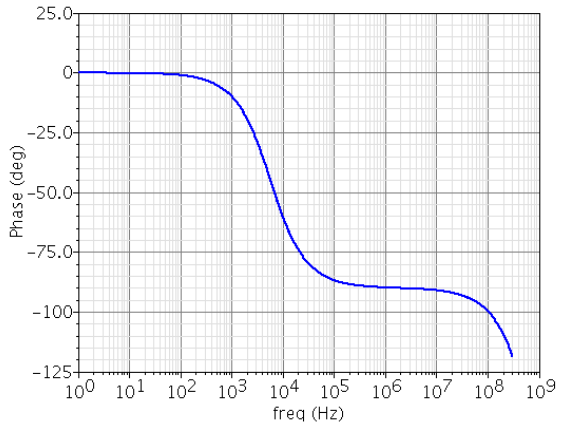
Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×5µm/0.18µm	$(W/L)_{17,18}$	2×10µm/0.36µm
$(W/L)_{2a,2b}$	1×25µm/0.18µm	$(W/L)_{19,20}$	2×40µm/0.36µm
$(W/L)_{3a,3b}$	50µm/0.18µm	$(W/L)_{21,22}$	2×10µm/0.36µm
$(W/L)_{4a,4b,4c,4d}$	1×12.5µm/0.18µm	$(W/L)_{23a,23b}$	1×10µm/0.18µm
$(W/L)_{5,6}$	1×20µm/0.18µm	$(W/L)_{24b,25b}$	1×10µm/0.18µm
$(W/L)_{7,8}$	1×60µm/0.18µm	$(W/L)_{24a,25a}$	3×10µm/0.18µm
$(W/L)_{9,10}$	1×60µm/0.18µm	C_a, C_s	0.8 pF
$(W/L)_{11,12}$	2×15µm/0.36µm	R_1, R_2	150 Ω
$(W/L)_{13,14,15,16}$	2×10µm/0.36µm		

Table 2: Comparison of the proposed method with existing methods for the two-stage op-amp.

Specifications	This work	[15]	[16]
DC-gain (dB)	93	93	93
Total runtime (s)	1549	1866	1722
Layout Area (mm²)	0.021	0.023	0.024
Area Utilization (%)	89	82	78



(a)



(b)

Figure 8. Bode plots of the two-stage operational amplifier: (a) magnitude response, (b) phase.

5 Conclusions

This paper presents a comprehensive and innovative approach for the automatic layout generation of analog integrated circuits, addressing the traditionally challenging and labor-intensive task of manual geometric constraint extraction. By integrating convolutional neural networks with transfer learning, specifically utilizing a fine-tuned pre-trained SqueezeNet model, the proposed method effectively identifies and extracts key geometric constraints such as symmetry and proximity directly from schematic images. This eliminates the need for manual intervention, thereby reducing design time and potential human errors. For the routing phase, a multi-objective optimization framework based on the non-dominated sorting genetic algorithm III was employed to simultaneously minimize critical layout metrics including wire length, via count, and arch segments. To enhance the efficiency and quality of solutions, a differential evolution algorithm was introduced for generating a high-quality initial population for NSGA-III, which accelerated convergence and improved optimization outcomes. The methodology was validated on the layout design of a two-stage operational amplifier implemented in a 0.18µm CMOS technology with a 1.8 V supply voltage. Simulation results conducted in MATLAB and subsequent verification in Cadence demonstrate that the proposed approach significantly outperforms conventional manual and automated layout techniques. Improvements were observed in layout compactness, performance metrics, and the level of automation, highlighting the potential of this method to streamline and advance analog IC design processes.

Ethical Considerations

All procedures performed in this study were under the ethical standards.

Acknowledgments

Authors thank all who helped us through this study.

Conflict of Interest

The authors report no conflict of interest.

Funding

According to the authors, this article has no financial support.

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